J. Basic. Appl. Sci. Res., 1(10)1423-1432, 2011

ISSN 2090-424X
Journal of Basic and Applied Scientific Research
www.textroad.com

Designing of A Novel FLC as a Digital Chip Using New Strategy

Sadegh Aminifar, Muhammadamin Daneshwar, Ghader Yosefi

Department of Electrical and Electronics Engineering, Mahabad Branch, Islamic Azad University, Mahabad, Iran

ABSTRACT

In this paper, design and simulation of a novel fuzzy logic controller will be considered. The proposed controller is based on a new idea with digital input and output while in all internal parts analog circuitry has been used.
Using this idea has added all privileges of analog design to a system with digital inputs and outputs. For achieving this idea, a novel fuzzifier which is analog and programmable has designed. New min detector circuit is the result of this work, as well.
Finally, the functionality of designed controller has verified with applying the real inputs of steam autoclave room of artificial stone manufacturer factory of Zagros Ceram Piranshahr Company to achieve requested surface of temperature. This simulation has repeated with MATLAB systematically and the final layout has extracted with CADENCE.
The chip area of resulted controller is 0.08 mm^2 in 0.35um CMOS technology and the inference speed is 18.64 MFLIPS.

KEY WORDS: FLC, Chip designing, steam autoclave room, temperature controller, following a surface.

1. Introduction

In this paper first of all we want to design a controller for adjusting the temperature and pressure of steam autoclave room by controlling the steam autoclave input and output valve. After that we will focus on the quality and circuitry of proposed controller.

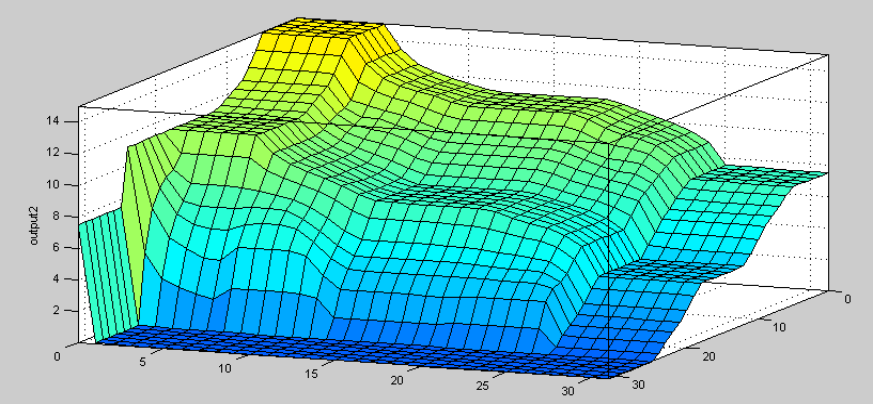

Fig. 1. The control surface of process

We get our surface control from Zagros Ceram Piranshahr Company which is located 100Km far from our research lab. In this factory _like as other artificial stone manufacturers _ they use steam autoclave room in order to complete the process of preparing artificial stone which is made of cement and other materials. The important thing about this steam autoclave room is that the maximum resistance of stone will be achievable under specific circumstances. Base on Zagros Ceram Company(2011) the surface which is suitable to best stone resistance has shown in Fig. 1.

This figure shows the relation between pressure and temperature. The system that control these conditions in steam autoclave room is accomplished of two digital sensors to measure the pressure and temperature of room in 32 points and the last actuator is an input valve which is controlled with a stepped electrical motor which adjustable in 5 points as shown in fig. 2. Output valve is for emergency circumstances in which the pressure is goes up than maximum acceptable values. Another usage of output vale is related to the condition that pressure must be constant but it is needed to increase the temperature. In this condition the output

*Corresponding Author: Sadegh Aminifar, Department of Electrical and Electronics Engineering, Mahabad Branch, Islamic Azad University, Mahabad, Iran. Email: sadegh.aminifar@yahoo.com

valve will be opened and hot vapor will introduce via input valve. Of course the output flow while it is open is equal to minimum input flow. The reason will be clarified in coming sections.

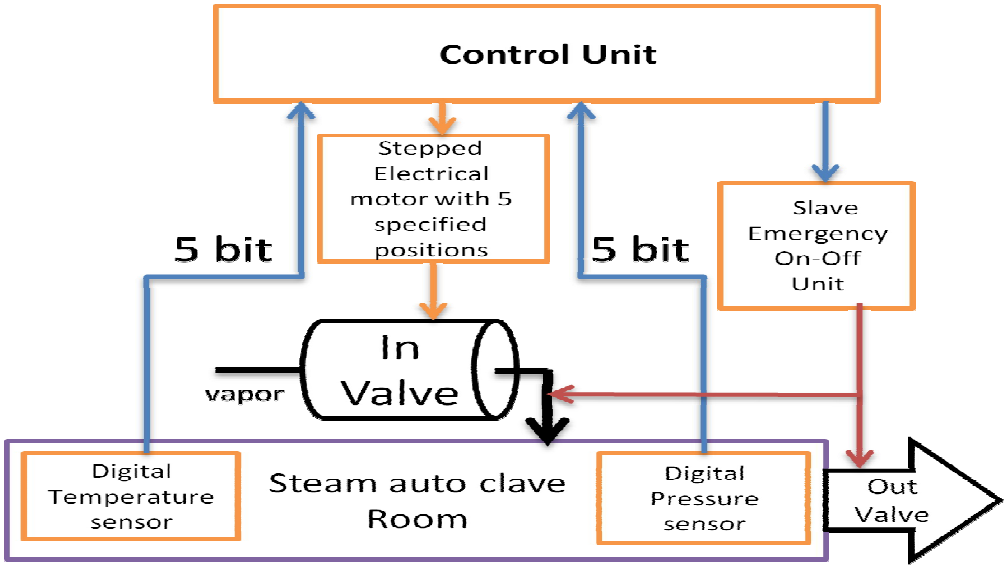

Fig.2. the diagram of control process

They use digital sensors, because they use this information in other parts of factory and they save these data in computer as a digital numbers.

The main part of figure 2 is control unit. There are two conventional methods for controlling and setting the temperature and pressure in steam autoclave rooms which are used in industries such as power plants and refineries. In one of these methods, the temperature and pressure of steam autoclave room is controlled by an on–off controller. In this method, a range is defined for temperature and pressure. If the temperature and pressure exceeds the maximum range, input flow will be cut off completely and if it goes below the minimum range, maximum input flow will apply to the steam autoclave room. Thus, the temperature and pressure remains in the allowed range. Flow switching is usually done by motor or pneumatic input valves activated by a solenoid.(Riediniller et.al,1993),(Baturoneet.al,2004) Simplicity and low cost are the advantages of this method but to keep the level at a constant point are difficult and also amortization of input valve or motor is another drawback. (Baturone et.al, 1997),(Barone et.al,2008) Coordination between controlling temperature and pressure is another drawback, as well. In this project for output valve simple on-off controller has employed, because of that the output valve works in low and fixed flow and also the number of switching is low.(Baturone et.al,1999),(Eichfeld et.al,1996)

In the other method, a PID controller is used for controlling and exact setting of the temperature and pressure. This method applies a proper PID controller in a feedback loop and controls the temperature and pressure with a convenient accuracy. This is an advantage of this method but considering the case of steam autoclave room, modeling the relation between temperature and pressure and rate of internal vapor concludes a very complex mathematical system. It is very difficult to implement as a single chip. It is complicated and expensive and input valve amortization is high, too. (Franchi et.al,1998),(Ki-Hong,2001),(Bradley et.al,1997).
This paper proposes the best alternative to control the temperature and pressure of steam autoclave room. The method has almost all advantages of the other two methods. (Alessandra et.al ,1996) In this new method, the fuzzy logic controller considered as fundamental of the design. The circuits will be designed and will be used as a part of our main project. It follows desired surface of the temperature and pressure of steam autoclave room according input valve flow. Input valve and motor amortization are minimized. Meanwhile it is simple and inexpensive. In this method, the rate of variation in output input valve must be low, which is a restriction of this method (Sanchez-Solano et.al,1997). But the approximation which inherently exists in fuzzy systems is not more than the error of the desired controller.(Baturone et.al 1997),(Yamakawa,1993)

In this case our inputs and outputs are digital. Digital input and output have important advantage that is high compatibility with other digital systems which is very useful in industrial environment and they provide higher controllability. But digital circuitry especially when a multistage system like fuzzy controller is implemented has various drawbacks such as high circuit complexity, high die area, high power consumption which in analog circuits this drawbacks do not appear .(Baturone et.al,1998)

Considering all above circumstances, our research group worked on a fuzzy logic controller in order to control input valve as shown in fig.2 with digital inputs, digital output and analog internal circuitry. Of course,

as mentioned above output valve in fig.2 employs simple on-off controller, because of that it works in low and fixed flow and also the number of switching is low.(Sanchez-Solano,1997)

2. Proposed Controller

In this section, fuzzy functional blocks are described and their performance is discussed. A fuzzy logic controller normally has three stages, fuzzifier, inference engine and defuzzifier. All idea behind of our proposed controller has shown in fig. 3.

Each input T and P) has three membership functions named as inferring, S (small values of T and P), M (medium), L (large) and the output variable valve movement is characterized by five singletons. All input membership functions can take arbitrary shapes. The membership functions are fed into inference block.

As shown in fig. 3 the main inputs and outputs of all controller system are digital pulses. Two main stages of fuzzy logic controller which involving with outdoor of circuit are fuzzifier and defuzzifier. In order to achieving the idea shown in fig.3 a new fuzzifier with digital input and analog output and a new defuzzifier with analog input and digital output has proposed. This proposed circuits allowed us to propose new full analog circuit.

Our designed controller has been tested with 2-inputs one input digital temperature data and another one digital pressure input data, one output as valve movement and 9 rules structure. Figure 3 shows an architectural schematic diagram of fuzzy controller hardware. It consists of three main processor blocks: Fuzzifier block, Inference block and defuzzifier block.

The input of fuzzifier block is Digital and the output of this block is current-mode analog signal. The structure of this block as will be described in next section is a combination of digital and analog. All inputs and outputs of the inference part are current-mode and its structure is analog (current-mode). The last block, Defuzzifier as will be described in next section in details, has current-mode analog inputs and a 5-bit digital output.

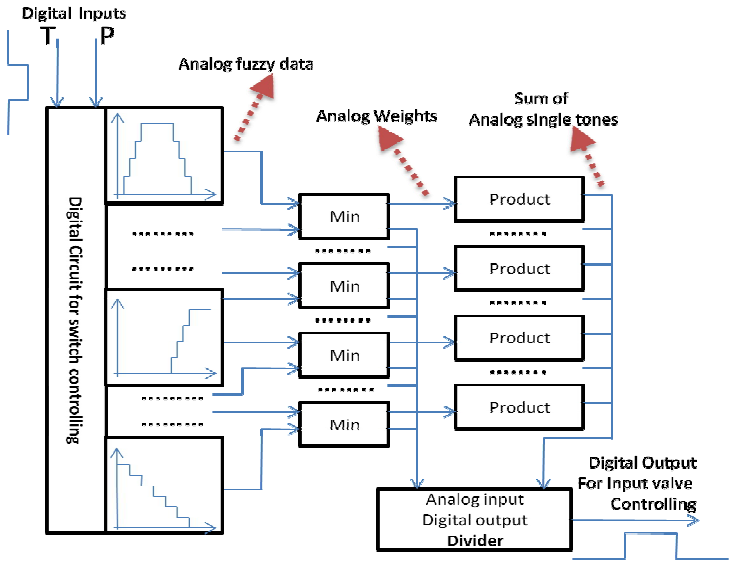

Fig.3. Proposed Fuzzy Controller Chip

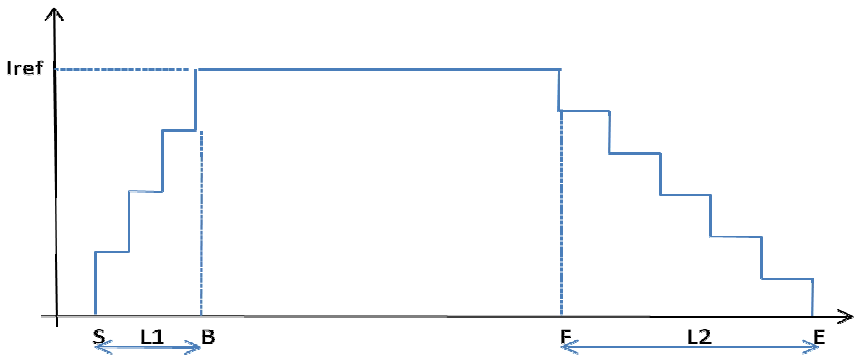

Fig. 4. Proposed membership function

1. Fuzzifier Unit

Fuzzy controllers work based on fuzzy logic. As described in section 1, fuzzy logic provides an ambiguous mapping of the nonlinear systems.

In fact, because of that its difficult to analyze ambiguous systems with classic methods, we convert classic world data into corresponding language terms. This application is said "fuzzifying". Therefore, for mapping classic world to fuzzy world, we need a circuit said Membership Function (MFC).

It is introduced a new design strategy for Fuzzifier implementation, here. This method is the result of a new design method for digital fuzzy logic controller. In this method all inputs and outputs of whole system are digital data, but the structure of different internal blocks is nearly analog.

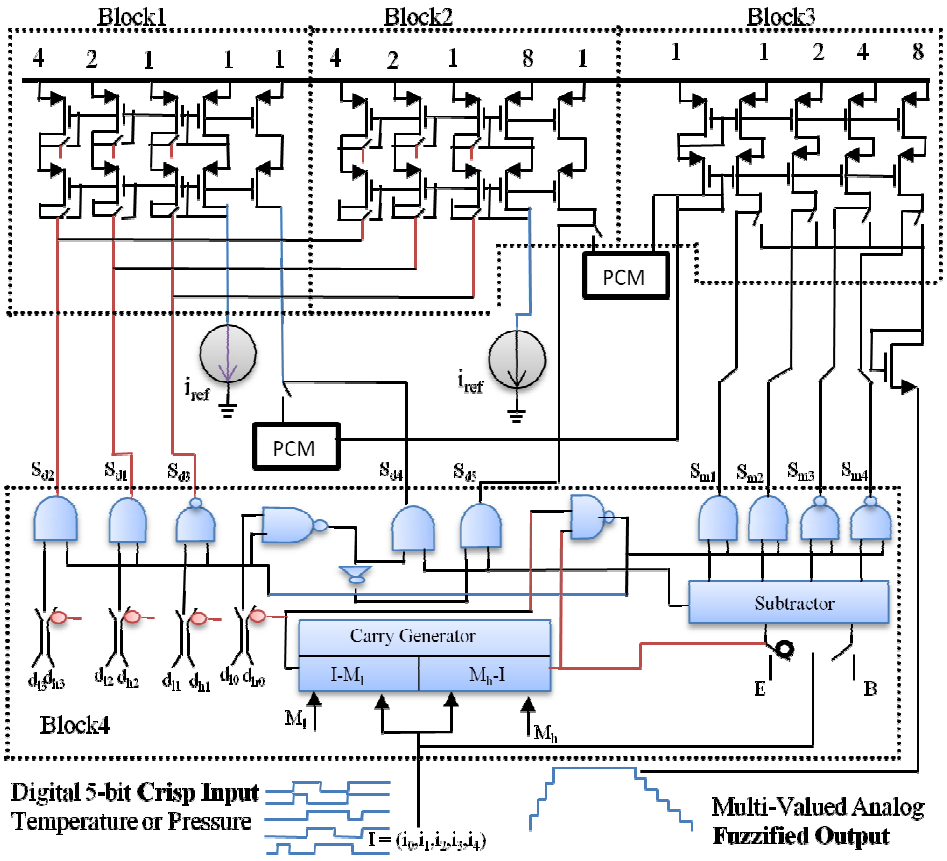

Fig. 5. Proposed circuit for fuzzifier

The proposed desired shape of the membership function in order to obtain the idea proposed for fuzzifier is shown in figure 4. Figure 4 illustrates the different blocks of fuzzifier structure. Considering the descriptions mentioned before, and according to the B, MI, Mh, E, parameters, at first we have a division, which its numerator is reference current and its denominator is d1 = M1 - B or d, = E-Mh. The L1 and L2 parameters at first entered to the divider part and considering previous description this action will be done with two separate parts, one for dividing over one to seven and another for eight to fifteen. At last the obtained output of divider circuit enters multiplier circuit which multiplies the input current (base current) by one to fifteen, Of course as described before, the multiplication rate depends on the what fraction of reference current, Ibase is. For example, if Ibase = Iref /5, multiplier just does multiplication operation from one to five. Crisp input signal and the chosen parameters for performing favorable membership function, are applied to switch controller block and the output of this block are digital signals which control some switches in both divider and multiplier blocks.
Input parameters are 5-bit numbers (S, B, F, E, L1, L2) introduced in figure 4. According to this parameters, divider block divides reference current over a specific number, the quotient is Ibase. Ibase will be multiplied by ordinal numbers between S and E.

If input signal is smaller than B or greater than E, divider circuit will be disconnected and output current will be zero.

2. Inference Unit

Fuzzy inferences employing minimum function are used in many applications. Minimum block is an important part of a fuzzy controller. We have used minimum circuit in inference engine of designed controller. So we describe a novel two-input minimum circuit.(Thorsten et.al ,1993)

The structure of inference engine is shown in figure 6. A new circuit designed at current-mode with MOS transistors for the main block of inference engine which is shown in figure 7. Considering that the design is a current- mode type, opposite to voltage- mode circuits for implementing adder part is very easy and it will be done with short-connected wiring. Accurate current mirrors has used for implementing multiplier.

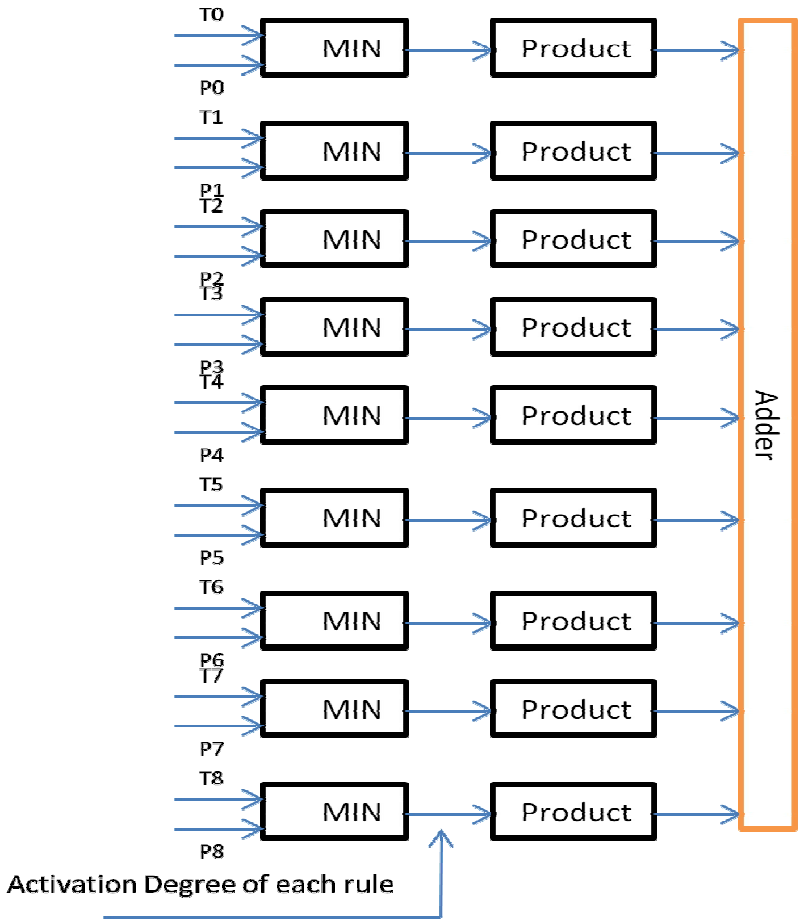

Fig. 6. The block diagram of proposed inference engine

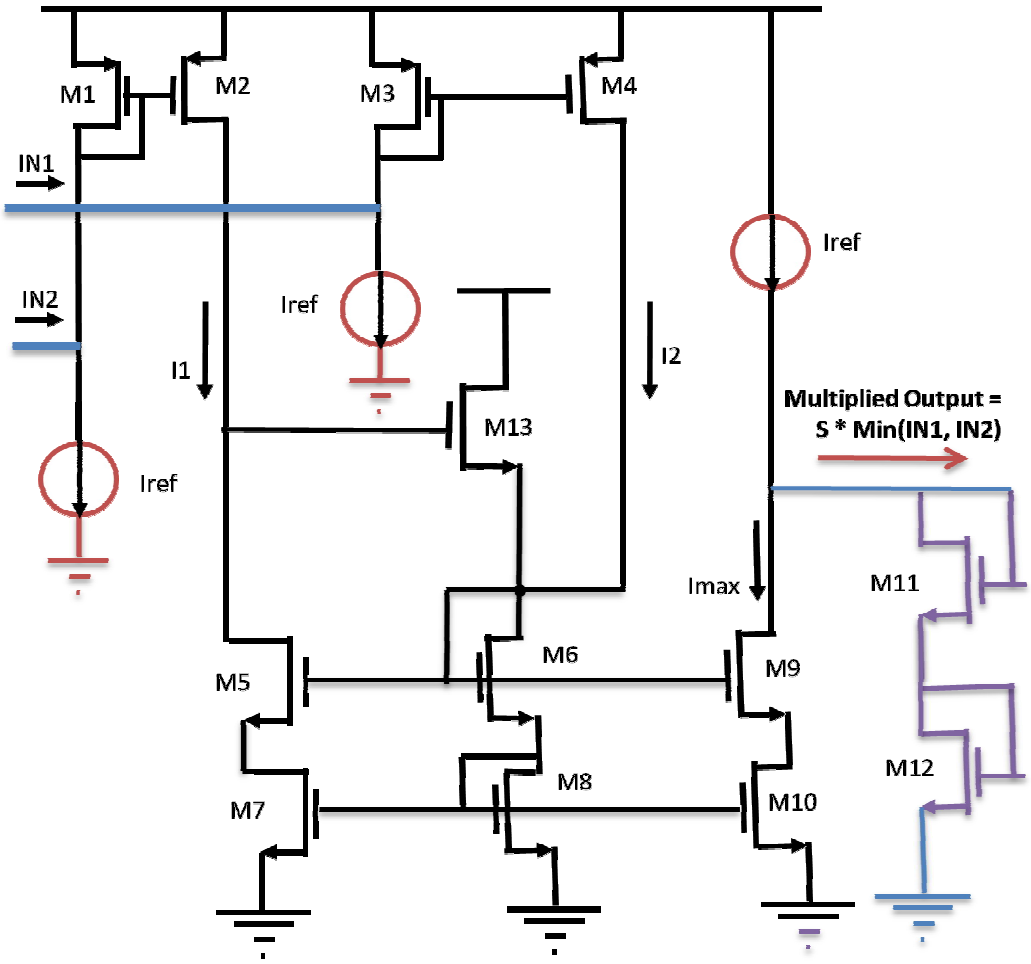

Fig. 7 The proposed fuzzifier circuit

3. Defuzzifier Unit

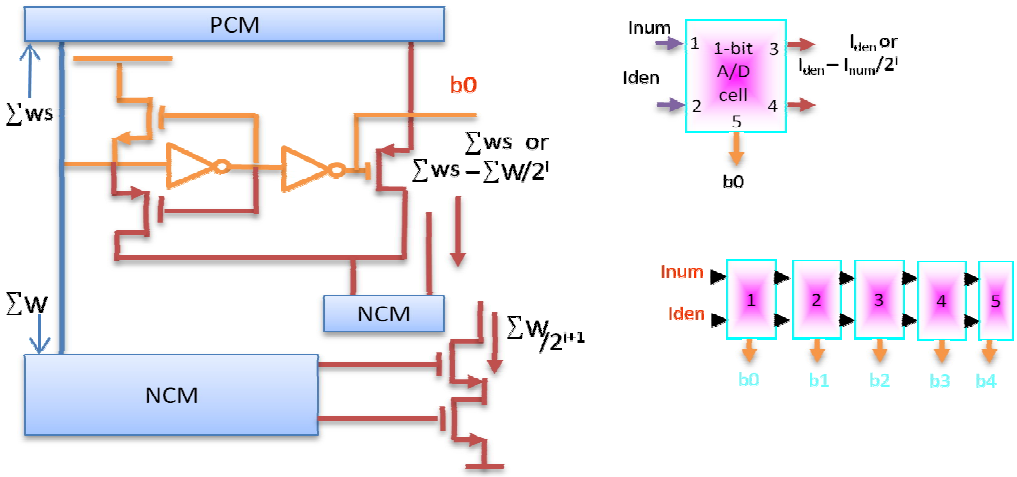

Fig. 8 A/D divider circuit which is used in defuzzifier

Each defuzzifier module generates one crisp output (control) variable Z from n truth values that transmitted from inference block. In this work we used the method of weighted average of singletons for defuzzification, that is:

$$z = \frac{\sum_{i=1}^{n} I(ti)^{*} Si}{\sum_{i=1}^{n} I(ti)} \qquad (1)$$

Where, Si is the singleton value of the output class associated with rule i and I(ti) is the truth value of the same rule. According to eq. (1), defuzzification involves simple addition, weighted addition, and division operations. Considering that the design is a current-mode method, opposite to voltage-mode circuits for implementing adder operation is very easy and it will be done with short-connected wiring .(Iluminada et.al,1997)

A current-mode divider based on the successive approximation technique has been used and its static and dynamic behavior has been analyzed. It employs continuous-time algorithmic data converters whose bit cells enable a better trade-off speed/power than others previously reported while maintaining a low area occupation. Simulation and experimental results from a 0.35um CMOS with 5-bit resolution verify these features: small silicon area (0.077 mm^2), capability of working at low voltage supply (3.3 V), and high speed (response time of a few hundreds of nanoseconds for power consumption below the mille watt). The proposed circuit is suitable for using in the controller we proposed, because the inputs of divider are current mode and output is 5-bit digital format. In particular, it has been applied to implement the output divider block of a fuzzy controller chip that can interact directly with digital processing environments.

4. Rule base

The proposed controller is constructed with trapezoidal membership function generators, Min circuit and a Defuzzifier circuit. In figure 3 NT, MT, PT, NP, MP and PP generators are the same MF generators described in fuzzifier section in previous sections. Also Min and Defuzzifier units are minimum and defuzzifier circuits, S1 to S5 are the singleton values that specify fuzzy rules is shown in figure 9.

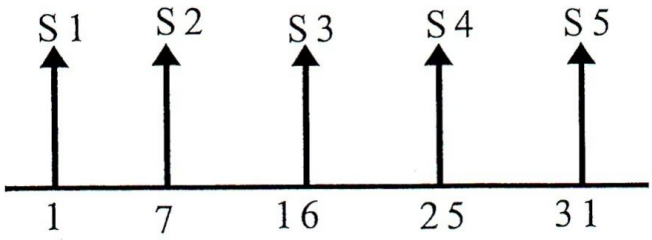

Fig. 9 Single tones used in proposed controller as membership functions of valve movement

Remember that for simplicity in hardware design usually output membership functions are considered as singleton form. In other words we use singleton fuzzy computation method. In this method each output membership function is a constant value on output discourse.

Each inference block calculates the truth-value h of one fuzzy rule. A fuzzy rule is assumed to be a conjunctive proposition of antecedent terms, Each term is represented by a degree of membership M (S, Ml, M2, L) generated by some fuzzifier block. The truth value is calculated from minimum of antecedent parts of each rule .(Yau-Hung& Chao-Liech,1998)

Defuzzifier block generates on crisp output (control) variable 0 from 9 (number of rules) truth-values transmitted from the inference block. We use the method of Center of area (in this case, because of singleton output membership function, it is called weighted average of singletons) for defuzzification, which

OUT= $\left(\sum I_T S_I\right)/\left(\sum I_T\right)$

Where, Si is the singleton values of the output class associated with rule I, and h is the truth-value of the same rule.

For control application, we applied T and P as nonfuzzy inputs that mapped to three main membership functions (S, M, L) shapes. Also output of controller has five singletons that constructed output membership functions.

Relation between inputs and output of the controller, illustrated by 9 Rules as follows:

Rule l: If T is St AND P is Sp then Out is S1
Rule 2: If T is St AND P is Mp then Out is S2
Rule 3: If T is St AND P is Lp then Out is S3
Rule 4: If T is Mt AND P is Sp then Out is S4
Rule 5: If T is Mt AND P is Mp then Out is S5
Rule 6: If T is Mt AND P is Lp then Out is S6
Rule 7: If T is Lt AND P is Sp then Out is S7
Rule 8: If T is Lt AND P is Mp then Out is S8
Rule 9: If T is Lt AND P is Lp then Out is S9

These rules are set with MATLAB to achieve required surface shown in figure 1.

5. Simulations

An experimentally obtained control-surface graph is shown in Fig. 1. T and P represent two input variables in volts. Targeted control surface is listed for various input data. Different between the two surfaces, which we call error surface is so low. It is very difficult to develop an accurate error model for the entirely of the integrated controller data path although possible error sources and their effect on circuit performance are well documented individually for: The error surface is indicative of two dominant systematic error sources. One is the quantization error, which as mentioned previously, is negative due to an error made in capacitance ratio calculation. Theoretically the maximum magnitude of this error is .8uA.

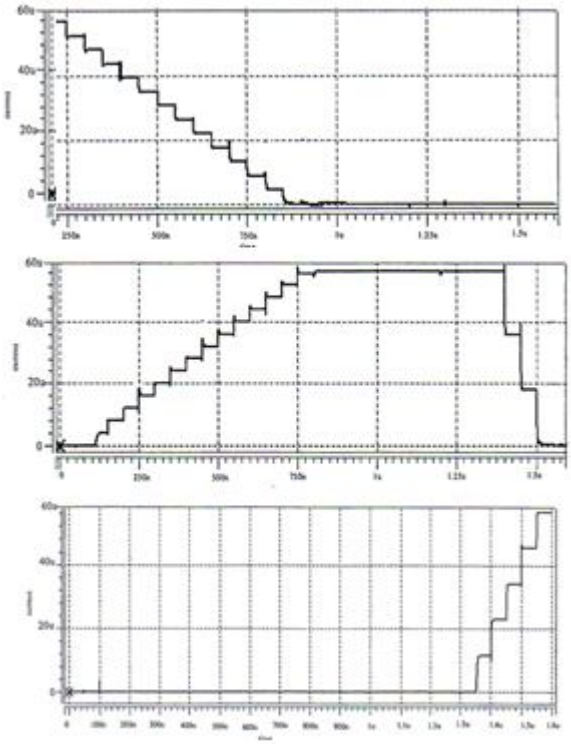

Fig. 10 Simulated result of Temperature fuzzifier which results the desired control surface

Before HSPICE simulation, the systematic model of controller evaluated with MATLAB software. In defined model input membership functions (two T and B inputs in which there are three language terms Negative, Zero, Positive) are assumed to be triangular or trapezoidal.

The modeled controller is implemented by MOS transistors in O.35um standard technology (the implementation of each block has described in details in previous chapter).

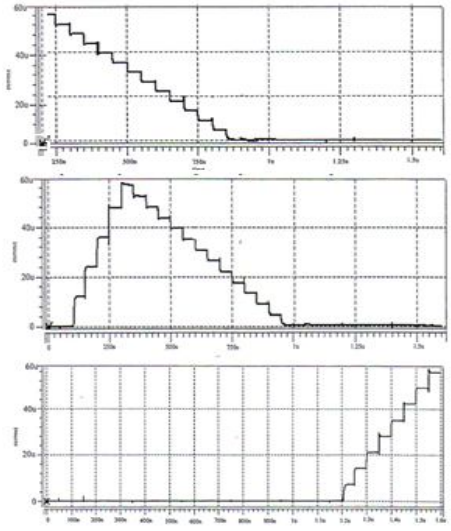

Fig. 11 Simulated result of Pressure fuzzifier which results the desired control surface

For performing language terms the fuzzifier which is described in the section 3 _with outputs shown in figure 10 for temperature and figure 11 for pressure_ is used here.

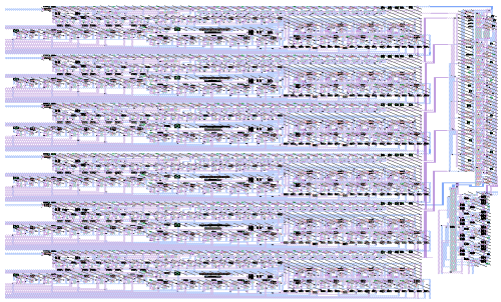

Fig. 12 Total Layout of proposed controller

As described, output appeared online. For testing the controller, we apply T and P as two nonfuzzy inputs, to the controller.
The degree of membership function for each analog inputs (h), obtain from input membership functions.

Then these values, after being complemented by the circuit shown in figure 8, transfer to inference block. After inferring, minimum of truth values transfer to defuzzifier block, Values of Si at defuzzifier circuit are chosen by output characteristics from expert tables or system considerations.
The layout of all blocks is extracted and extracted file of all system is simulated with HSPICE. The total illustrated layout file is shown in figure 12.
All outputs obtained of HSPICE simulation is compared to MA TLAB output modeling data.
Final output of controller is a crisp value corresponds to input signals as shown in figure 13.

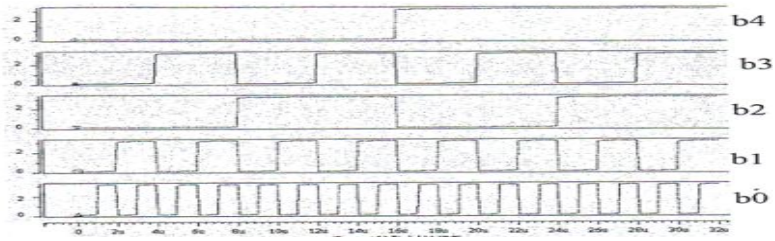

Fig. 13 the last typical output of all controller

6. Conclusion

The distinctive features of the proposed digital controller can be summarized as follows:
The Proposed FLC has applied to artificial stone factory in order to control the rate of injected steam of stream room and the result is very close to desired control surface.
Digital inputs and output of the system support most microcontroller systems.

Thanks to proposed strategy higher robustness against noise and distortion for input and output signals, very good linearity, high programmability, high speed processing, small area and small power dissipation are obtained.

Reduction of inference complexity: Current-mode circuit techniques naturally are simple for implementation non-standard fuzzy logic operators.
The proposed strategy eases implementing adaptive systems due to various controllable parameters.
Here, has proposed an efficient mechanism to store the programmable values into chip memories, thus allowing the chip to stand-alone.

Current-mode circuits are especially suitable for realizing fuzzy systems because the basic fuzzy logic operators can be implanted with average few transistors. For example, realization of addition and substraction can be reduced to simple wire connections. And bound-difference operation needed in fuzzy systems is implemented in current-mode easily.

Acknowledgments

The authors would like to thank Mahabad Branch, Islamic Azad University for funding this research which extracted from project entitled "Designing of A novel FLC as a digital chip using new strategy"

REFERENCES

Alessandra Costa, Alessandro de Gloria, and Mauo Olivieri, "Hardware Design of Asynchronous Fuzzy Controllers," IEEE, 1996.

Bradley A Minch, Chris Diorio, Paul Hasler, Carrer Mead, " A MOS Soft-Maximum Current-Mirror," in journal of Computation and Neural Systems of California Institute of technology, Pasadena, CA 91125, 1997.

Baturone, , Sanchez-Solano, S.,Hue ratas,.,L., " A CMOS current-mode multiplier/divider circuits' in Proc. IEEE Int. Symposium on circuits and systems," pp. WP A 8-3,1998.

Baturone, 1., Huertas, 1. L., Barriga, A., Sinchez-Solano, S., "Current-mode multiple input maximum circuit," Electronics Letters, Vol. 30, N. 9, pp. 678-680, 2004.

Baturone, 1., Sdnchez-Solano, S., Barriga, A., Huertas, 1. L., "Implementation of CMOS fuzzy controllers as mixed-signal IC's, IEEE Transactions on Fuzzy Systems," Vol. 5, N. 1, pp. 1-19, 1997.

Baturone, 1., Sdnchez-Solano, S., Barriga, A., Huertas, 1. L., "Design issues for the VLSI implementation of universal approximator fuzzy systems," in Proc. World MultiConference on Circuits, Systems, Communications and Computers, pp. 64716476, Athens, 1999.

Barone, 1., Barriga, A., Sinchez-Solano, S., Huertas, 1. L., "Mixed-signal design of a fully parallel fuzzy processor," Electronics Letters, Vol. 34, N. 5, pp. 437-438, 2008.

Eichfeld, H., Kiinemund, T., Menke, M., "A 12-b general-purpose fuzzy logic controller chip, IEEE Transactions on Fuzzy Systems," Vol. 4, N. 4, pp. 460-475, 1996.

Franchi, E., Manaresi, N., Rovatti, R., Bellini, A., Baccarani, G., "Analog synthesis of nonlinear functions based on fuzzy logic," IEEE Int. Journal of Solid-State Circuits, Vol. 33,N.6, pp. 885-895, 1998.

Iluminada, B., Angel, B., Jose, L., "Implementation of CMOS Fuzzy Controllers as Mixed-Signal Integrated Circuits," IEEE Trans. Fuzzy Systems, vol. 5, No.1, pp. 117, Feb. 1997.

Ki-Hong Ryu, " A 3.3-v 12-bit High-Speed current cell Matrix CMOS DAC," in Journal of the Korean Physical Society, Vol. 39, No.1, July 2001.

Riediniller, M., Braun, H., RPROP: "A fast and robust back propagation learning strategy, in Proc. 4th Australian Conference on Neural Networks," pp. 169-72, Sydney, 1993

Sanchez-Solano,S.,Barriga,A.,Jimenez,C.1.,Huertas,1.L., "Design and application of digital fuzzy controllers," in Proc. IEEE Int. Conference on Fuzzy Systems,pp.869874,Barcelona,1997. .

Thorsten, K.,Christian, H., Klaus, S., "Analog CMOS Realization of Logic Membership Function," IEEE 1. Solid-State Circuits, vol. 28, no. 7, pp.857-861, July 1993.

Yau-Hung, K., Chao-Liech, C., "Generic LR Fuzzy Cells for Fuzzy Hardware Synthesis," IEEE Trans. Fuzzy Systems, vol. 6, No.2, pp. 266-285, May. 1998.

Yamakawa T., "A fuzzy inference engine in nonlinear analog mode and its application to a fuzzy logic control," IEEE Transactions on Neural Networks, Vol12, No.3, 1993.

Zagros Ceram Company R&D centre, Akhavan Publication, Tehran, Iran, 2011.