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A Novel Defuzzifier as a Result of Designing of a Fuzzy Logic Controller as a Digital Chip Using New Strategy

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ABSTRACT

In this paper, design and simulation of a novel defuzzifier applicable in a fuzzy logic controller will be considered. The proposed controller is based on a new idea with digital input and output while in all internal parts analog circuitry has been used. The proposed defuzzifier enables a better trade-off speed/power than others previously reported in the literature while maintaining a low area occupation. The resulting divider circuit offers a low voltage operation, provides the division result in digital format, and it is suitable for applications of low or middle resolution like applications to fuzzy controllers. The analysis is illustrated with Hspice simulations and the results from a CMOS divider prototype with 5-bit resolution. The results from a CMOS voltage-mode fuzzy controller chip that contains the proposed design are tested successfully. The final layout is illustrated and extracted.

Keywords: Defuzzifier, fuzzy controller, voltage-mode circuits, hierarchical strategy

I. INTRODUCTION

Before starting the proposed defuzzifier, many hardware realizations of defuzzifiers have been studied which are used to address the hardware implementations of fuzzy logic controllers. The first hardware implementation of the fuzzy processor was done by Togai and Watanabe (Watanabe,H., et al, 98) (MontazerZamanoddin, et al, 2005). Watanabe improved the performance of the fuzzy logic controllers by proposing a dynamically reconfigurable and cascade architecture. A fuzzy processor using SIMD was proposed by Baturone (Baturone, l., et al, 98) (Baturone, 1., et al, 97) and (E. H. Mamdani, et al, 98). A bit scalable architecture of fuzzy processors is proposed by Fuller (Fuller, R. 2002). This architecture is suited for automatic synthesis of digital fuzzy controller. G. Ascia et al. proposed a rule driven fuzzy processor to address some real time hardware issues. They also proposed VLSI architecture for fuzzy inference that includes rule chaining (Gam Ali Mazer, et al, 2010) and fuzzy expert system for traffic in ATM network. (Jeeoon-ShiongWanog; et al, 2002) designed a simple and power efficient fuzzy logic controller and achieved a speed of up to 6 MFLIPS.

In the method COA thanks to geometric mean, we will arrive to the very exact defuzzified output. But normally this method involves with more complex circuitry.

I. The main techniques used for implementing dividers in fuzzy controllers

A divider circuit is usually required in the fields of analog signal processing and parallel computing fuzzy systems. In this issue, we will focus on the application to digital fuzzy logic controllers, which are proposed in this project.

Typical fuzzy system that we have proposed here, infer a crisp (not fuzzy) output by aggregating all the rules' conclusions and performing a division. One of the main problems that appear when implementing a fuzzy system in hardware is the selection of an adequate divider circuit. The divider is usually the circuit that limits the speed, precision and interface capabilities (it is the output block) of the resulting fuzzy chip. Several techniques to design divider circuits have been proposed in the (Zhojian, L., et al, 90). Conventional log-antilog or bipolar Trans linear techniques have been employed in the analog fuzzy chips described in (S. Aminifar, 2010). These structures can be realized with CMOS technology by using MOS transistors working in sub threshold region. However, the low voltage levels make them operate slowly (S. Aminifar, 2010). Low operating speed is also the main limitation of the dividers based on the time-division technique (Zhojian, L., et al, 90). The MOS Tran linear principle is another approach. In this case, the main limitation is a low resolution because the performance of the resulting circuits is very sensitive to deviations from the simple square-law model of the transistors in saturation, caused by length-channel modulation, mobility reduction or mismatching.

Another technique widely employed is to invert the behavior of a multiplier by using local feedback or by inserting it in the feedback path of an inverting amplifier. Performance of this divider depends primarily on the

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performance of the amplifier employed. Precision is mainly limited by offsets associated with the input and output variables. The analog fuzzy chips reported in (Sanchez-Sinenico, E., et al, 99) contain this type of dividers.

II. Defuzzifier Circuit

Each defuzzifier module generates one crisp output (control) variable Z from n truth values that transmitted from inference block. In this work we used the method of weighted average of singletons COA for defuzzification, that is:

$$z = \frac{\sum_{i=1}^{n} I(ti)^{*} Si}{\sum_{i=1}^{n} I(ti)}$$

Where, Si is the singleton value of the output class associated with rule i and I(ri) is the truth value of the same rule. According to above question, defuzzification involves simple addition, weighted addition, and division operations. The adding operation is very easy and it obeys simple ohm's rule which is illustrated in figure 1. (AliyonterAlidasank, 2000)

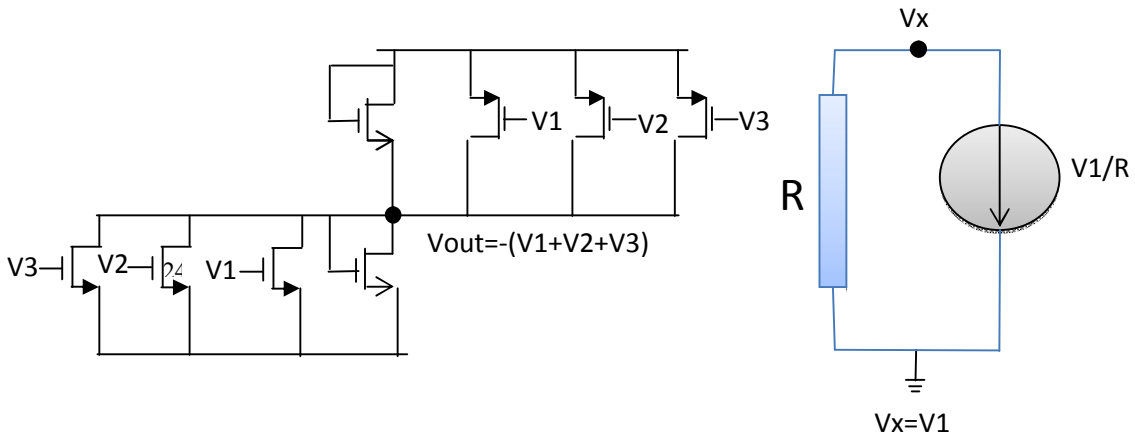

Fig. 1: Adder circuit and adder principal used in proposed defuzzifier

III. Divider Unit

A voltage-mode divider based on the successive approximation technique has been used and its static and dynamic behavior has been analyzed. It employs continuous-time algorithmic data converters whose bit cells enable a better trade-off speed/power than others previously reported while maintaining a low area occupation. Simulation and experimental results from a 0.35um CMOS with 5-bit resolution verify these features: small silicon area (0.088 mm^2), capability of working at low voltage supply (3.3 V), and high speed (response time of a few hundreds of nanoseconds for a power consumption below the mille watt). The proposed circuit is suitable for using in the controller we proposed, because the inputs of divider are voltage mode and output is 5-bit digital format. In particular, it has been applied to implement the output divider block of a fuzzy controller chip that can interact directly with digital processing environments.

Divider circuits are usually required in the fields of analog signal processing and parallel computing fuzzy systems. In particular, this issue focuses on the hardware implementation of a digital fuzzy controller, where the divider circuit is usually the bottleneck.

Divider circuits can be implemented with digital blocks but it takes a very complex digital circuitry. An efficient design based on voltage-mode data converters is presented herein. Continuous-time algorithmic converters are chosen to reduce the control circuitry and to obtain a modular design based on a cascade of bit cells, which work with analog voltage mode inputs and digital signal output.

IV. Used algorithm to implement divider block

Used algorithm for implementing successive algorithm is shown in figure 2.V_{den} is the sum of inference line outputs and V_{num} is the voltage which is the sum of weighted values of inference output.
In figure 2 pin 1 is the voltage which is the sum of weighted values of inference output ($w_1*S_1 + w_z*s_z + \ldots$) and pin 2 is

the voltage which is the sum of truth-values of rules ($W_1 + W_z + W_1 + ...$). Pin 3 and 4 are voltage outputs which are produced to apply to similar next cell. Pin 5 is digital output of the cell.

The ADC converter employed are coupled in the sense that they begin conversion by the same bit (the most significant bit, MSB) so that the digital outputs are provided after only one stage.(as illustrated in figure 2.)
Besides, the response time can be smaller than N times the duration of the slowest operation because continuous-time data converters are employed.

The most efficient of the divider circuits enables realization of small and fast divider circuits suitable for applications of low or middle resolution (below 9 bits, which is higher than the resolution obtained by many of the above commented proposals). Performance of the used divider circuit is illustrated with Hspice simulation and has been verified with 0.35um CMOS prototype with 5-bit resolution.
Among the different designs of voltage-mode converters, algorithmic types are rarely used but in this paper we used it very simply and design can be implemented. The data converter also consists of a cascade of 5 bit cells but no control circuitry is required to govern the signal transmission from one cell to another. Besides, the response time can be smaller than 5 times the duration of the slowest operation. Because of that the converters are sensitive to mismatching among the cells, so that resolution is limited typically to 5 bits.
Considering applications of low or middle resolution like IC realizations of fuzzy controllers, we have selected continuous-time algorithmic converters to reduce the control circuitry and the response time. The resulting divider circuit has the modular structure shown in Figure 1. Each bit cell contains an ADC bit cell that provides a bit of the digital output, {bi}. The output {bi} is the digital code of the voltage-mode division Vnum/Vden. Design considerations for the ADC bit cell is given in the following.

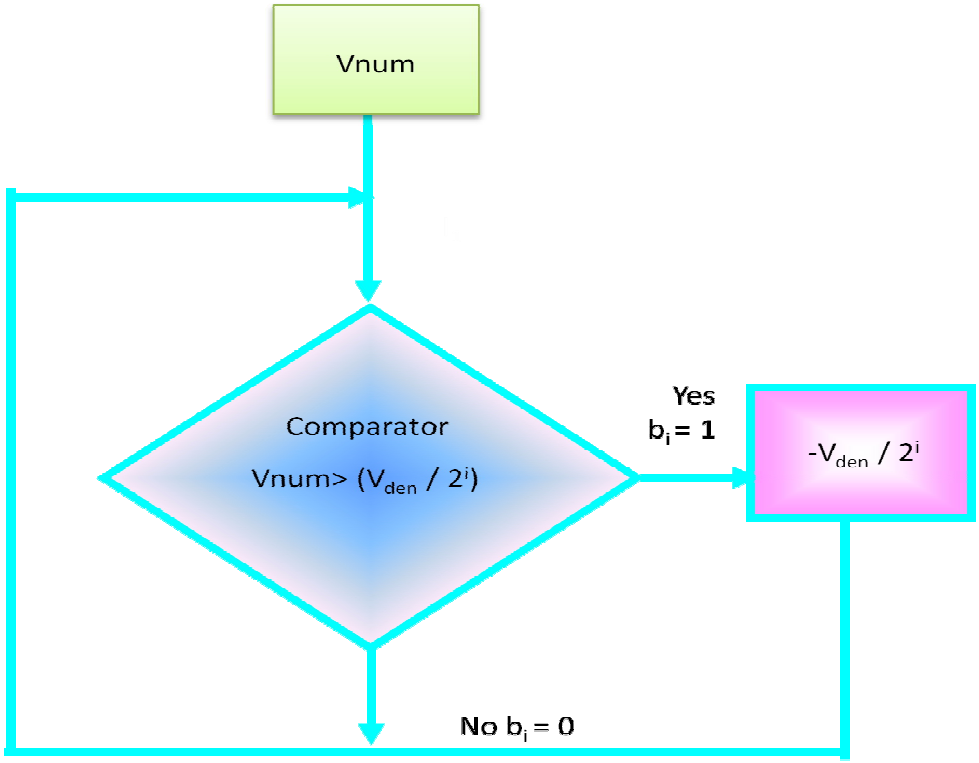

Fig. 2: Flow chart of the dividing algorithmic conversion method

V. Design considerations for the ADC voltage mode bit cells.

Most reported algorithmic ADC converters implement the multiplying algorithmic conversion in current mode. However, we applied the dividing algorithmic conversion in more suitable way for a divider circuit in order to have Vden as the full-scale voltage of the ADC converter. Focused on this case, the input range for Vnum is Vnum<Vden.
Using a voltage-mode approach, the operations required by an algorithmic ADC conversion are performed by voltage short circuit connections and voltage comparators.
In the following, we consider and discuss two structures of ADC bit cells that combine different circuit techniques to improve resolution and speed. These circuits implement the algorithm shown in the figure 2.
The bit bi is obtained from the comparison of Vnum with Vden /2i.
Since the input to this comparator is capacitive, the offset is virtually zero and resolution is not degraded. Hence, an ADC converter based on these cells can occupy less area than another's for a given resolution and range of operation.

Another advantage of these cells is that their speed is higher since the comparator employed is faster.

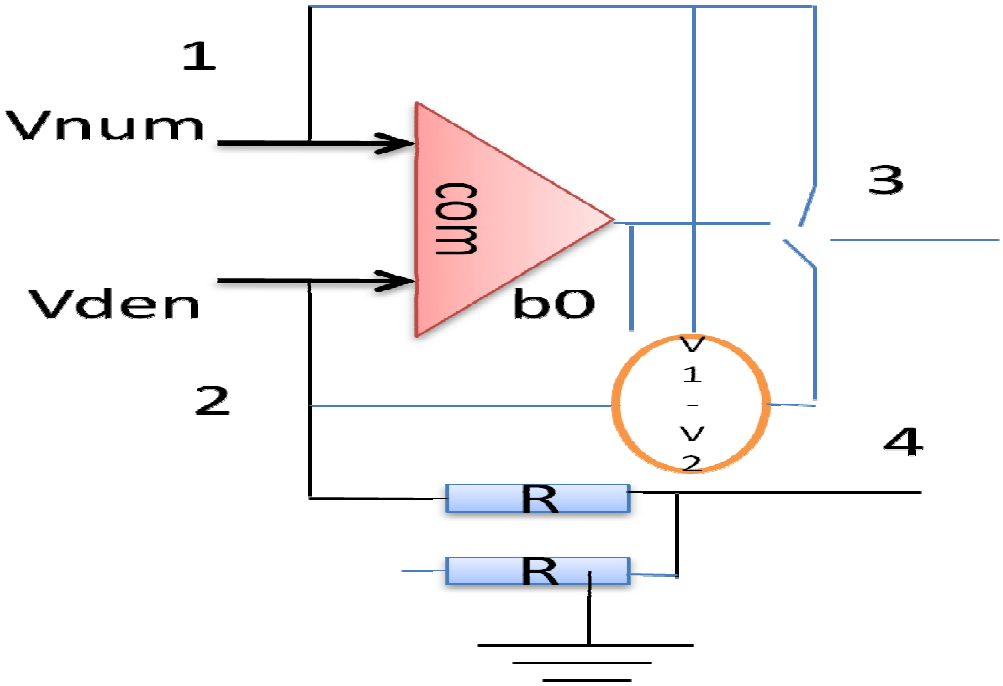

Fig. 3: Main blocks of ADC voltage mode cell

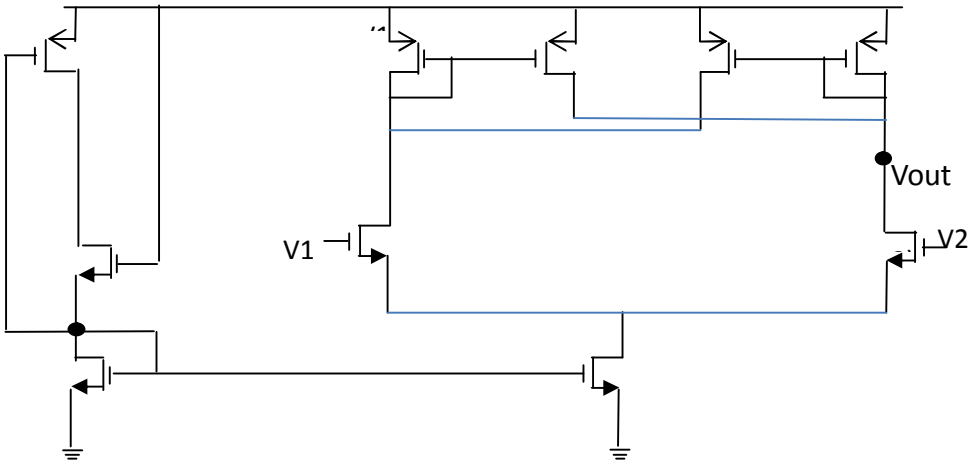

Fig. 4: Proposed Comparator used in 1-bit ADC

The comparator shown in figure 4 in the proposed structure works as below:

The voltage decrease induced at input nodes can make Vnum be momentarily superior to Vden /2i. Hence, bi can return to "1" if the comparator is too fast.

Glitches have to be reduced if high-speed operation is required. A solution is to include the active load feedbacks in Figure 4. This active load feedback is conducting when bi is "1", making low the voltage at output node. Therefore, a change of bi from "1" to "0" causes a momentary increment in the voltage at input node and, indirectly, at output node. Opposite to the above commented situation, this affirms the "0" value of bi.

VI. HSPICE Simulations of 1 bit ADC voltage mode Cell

Input of denominator and numerator changes from 0 to 3.3v. In this case the numerator is considered 1.65v. If denominator voltage is smaller than 1.65v, then output voltage will be zero, which is corresponding to logical zero. If denominator voltage greater than or equal to 1.65v, then output voltage will be 3.3v, which is corresponding to logical one.

The output voltage of the cell, which is applied to next successive cell, has the value of 1.65v for input voltage3.3v. It shows sufficient value for another four cells to create output with five bit resolution. The output voltage

of the cell which applies to next successive cell
ADC cell and its reflectance in the comparative node
Transient simulation of I-bit cell: Applying a voltage pulse in the range of 3.3v to the 1 bit ADC voltage mode cell, it results the outputs illustrated in figure 5 (numerator is set to
1.65v).

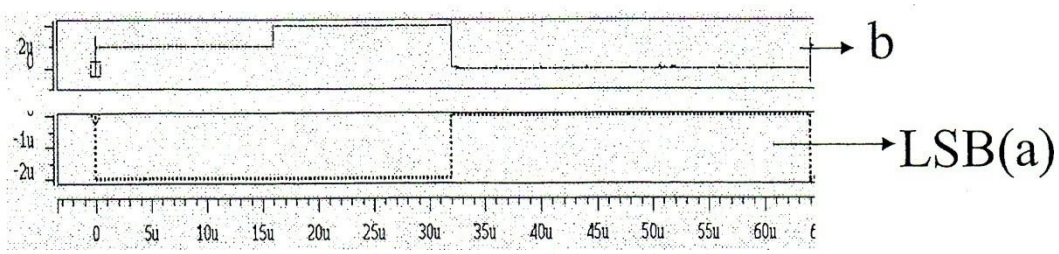

Fig. 5: Transient HSPICE simulation results (a,b)

Transient simulation of 5-bit hierarchical ADC cell: 1. First we applied a pulse as LSB (a) shown in figure 5to the hierarchical structure shown in figure 2 for the range of 3.3v.

The analysis is illustrated with Hspice simulations and the results from a CMOS divider prototype with 5-bit resolution. The results from a CMOS voltage-mode fuzzy controller chipthat contains the proposed design are tested successfully.

The main difference between the combined proposed method and the other methods which proposed for fuzzifier is that: in previous methods they use digital circuitry for increasing the flexibility of analog fuzzy logic controller, but hear analog circuitry used for increasing the speed and liability for implementing the COA method which has less sum squared error.

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