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Best Performance Parallel Prefix Adder Cells by Carbon Nano Tube Field Effect Transistors

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ABSTRACT

In this paper, a novel design technique for prefix adder cell based on CNTFETs with high speed is proposed and compared with previous design. This prefix adder provides low power consumption and high performance have been implemented by AND/OR/XOR gates. HSPICE simulations have been performed on 566 transistors at 0.9v VDD. Simulations results show the superiority in terms of power consumption and power delay product (PDP) in compare with the previous work.
Keywords: CNTFET, parallel prefix adder, nanotube.

1. INTRODUCTION

The invention of carbon nano tubes (CNTs) with respect to changes in circuit design is one of the greatest explorations Pages of Nano tubes of carbon atoms within the unit and wired networks, it is clear that the roller cover on one side move. Carbon Nano tubes are hollow pipes made of carbon sources such as gas or graphite with naphthalene, electrical discharge and etc. These tubes due to have vast special area (700-1000 gr/m^2), high solidity (50*iron solidity) and exceptional electricity and electronic particularly are used in many places. Their weight is 1/6 the weight of iron. The Nanotube conducts mainly on surface of the Nanotube where all chemical bonds are saturated and stabled; therefore, without careful passivation interface between the Nanotube channel and the gate dielectric, for example there isn't any equivalent interface silicon dioxide or silicon. Finally Schottky barrier with the metallic nano tubes is the dynamic switching component in inherent Nanotube devices (J. Appenzeller, 2008).This advantage causes that these tubes are first choice for constructing bridges, air planes and even spacecraft. Nano tubes are divided into two groups: Single wall and Multi wall. Single wall is more being used than multi wall due to simple production. Single wall Nano tubes are produced in three ways: Arc Discharge, Deposition or CVD Chemical Vapor and Laser Vaporization. We use transistors type of carbon Nano tube which is called CNTFETs.

2. CNTFETs

A CNT could be single-Wall Carbon NanoTube (SWCNT) or Multi-Wall Carbon NanoTube(MWCNT) (Jaldappagari Seetharamappa, Shivaraj Yellappa, and Francis D'Souza, 2006). SWCNTs are formed of a cylinder, while the MWCNTs are made over one cylinder of Carbon sheets. The electrostatic contacts between sheets, makes it possible to assume that the electrical characteristics of graphite are autonomous.
Depending on its chirality vector, a SWCNT could be visualized as a graphite sheet (a hexagonal lattice of carbon) which is rolled up and joined together:

$$C_h = n_1\overline{a_1} + n_2\overline{a_2} \quad (1)$$

Where [$\overline{a_1}, \overline{a_2}$] the reticulation unit vectors, the positive integers (n1, n2) are used to determine the chirality of tube. Generally, the generic diameters of Carbon Nanotubes are about several nanometers and many micrometers in length (A.P. Graham, G.S. Duesberg, W. Hoenlein, F. Kreupl, M. Liebau, R. Martin, B.Rajasekharan, W. Pamler, R. Seidel, W. Steinhoegl, E. Unger, 2005). The purpose of the C_h is the perimeter of the CNT. It is expressed according to:

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

d=1.44, Å is the distance of the inter-carbon-atom within the hexagonal network, and the lattice constant (a) could be computed based on:

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$$3d = 2.49\ \text{Å} \quad (3)$$

CNTFETs have three different types, Two kinds of CNTs have been studied more, to review Carbon Nanotube transistors(A.P. Graham, G.S. Duesberg, W. Hoenlein, F. Kreupl, M. Liebau, R. Martin, B.Rajasekharan, W. Pamler, R. Seidel, W. Steinhoegl, E. Unger, 2005).

The first type of CNTFET is schottky barrier that is consisted of metal-semiconducting NanoTube, that works on the principle of direct tunneling over on Schottky barrier at the joint of source-channel,and under the standard of direct tunneling through the schottky barrier operates then by nonideal contact between metal and carbon which is composed. The barrier width is modulated by applying a gate voltage and thus the Trans conductance of the device is depend on the amount of gate voltage. To dominate these limitations with the SB-CNTFETs, there have been efforts to implement new CNTFETs which have normal behavior like MOSFETs. In this MOSFET-like device, the on-current is defined by the quantity of charge that can be induced in the channel through the gate. It is evident that the MOSFET-like device will have the better performance in comparison with SB-CNTFETs. CNTs have banded gaps that depend on the nanotube diameter. The band gap is an amount of the threshold voltage (V_{TH}) of the CNTFET. In our work we have used the Principle that CNTs can be implemented to have demanded threshold voltages related on their diameter. The threshold voltage of the Carbon Nanotube channel is the follower of the diameter, which can be represented as:

$$V_{\text{TH}} = \frac{0.42}{d(nm)}V \quad (4)$$

The diameter of the Carbon Nanotube is obtained by the formula $\mathbf{D_{CNT=}C_h/\pi}$. Generally the generic diameters of Carbon Nanotubes are about several nanometers (A.P. Graham, G.S. Duesberg, W. Hoenlein, F. Kreupl, M. Liebau, R. Martin, B.Rajasekharan, W. Pamler, R. Seidel, W. Steinhoegl, E. Unger, 2005).

3. Previous Work

NanoTube field effect transistors (CNTFET) have been implemented by the carbon NanoTubes and their usage in the electronic switching. because of orbital parameters in CNTFET including high speed, low delay, and the similarity of their operation with MOSFET, low power consumption and PDP replaced by MOSFET transistors which are suitable for this type (A. Heung and H. T.Mouftah, 1985; J. Appenzeller, 2008). Delay of circuits that are designed with silicon-based transistors to integrate circuits using capacitors middle is very evident and due to the low efficiency of the entire circuit. Regarding the low efficiency of circuits which use capacitors, their speed will be reduced, and this is one of the problems with designing integrated circuits with silicon. Another major problem of this type of design is the size of CMOS transistor. We directed our research towards the necessity of using CNTFET transistors.

The items listed above in this article are to try to learn how to work with investigation of CNTFET transistors and CMOS transistors and also examine how this type of parallel prefix adder and previously a completely new circuit for prefix adder parallel design was presented for using CNTFET technology. Due to the large size of silicon transistors and also because of shrinking transistors of this type, many problems and limitations for integrated circuit designers are created. Therefore, the need was felt more than the using of CNTFET transistor. In early 1970, the designers of new technology designing and manufacturing of high-density circuits invented the NMOS. Given the problems of this type of technology in the same year, another technology was named as CMOS (Navi, K., Kazemi parsa, M. and Ghorbannia Delavar, A., 2005; Garg, A., Chan Carusone, A. and Voinigescu, S. 2006; Dayu Wang, Xiaoping Cui, Xiaojing Wang, 2011). Besides, adder circuits because of major part of the arithmetic logic unit, floating-point processors or special-purpose chips make up a very important part of the architecture (D.Harris and I.Sutherland, 2003; Tackdon Han and David A.Carlson, 1987). Therefore, no matter how quickly this type of collector is, excessive speeding is the whole circuit. On the other hand, the binary operation of arithmetic logic unit is one of the parallel prefix adder input bits in parallel with a fast and highly efficient solution to the problems of binary offers (K.vitoroulis, A.J.AI.Khalili, 2007). The issue of Ai and Bi is Parallel prefix adder circuits as inputs can be real or complex numbers, fixed or variable with time (Peter M.Kogge and Harold S.Stone, 1973). Collectors prefix derived from the collectors are expected to carry (P. Ramanathan and P T Vanathi, 2010). Smoked collectors are the most basic modules for architectural design and to investigate and review the results of this Parallel prefix adder and a general technique for increasing the operating speed are smoked (S.Knowles, 2001; Haikun Zhu, Chung-Kuan Cheng, Ronald Graham, 2005). In this new method we will use carbon nanotube transistors 566 and we will review the large number of transistors that can reach a good answer.

4. Proposed Parallel Prefix Adder

In this work a prefix adder cell are proposed based-CNTFET that implemented by 566 transistors with AND/OR/XOR gates. For XOR function, when both of inputs are similar, output should be '0' otherwise output should be '1'.for OR function, when one of the inputs is '1', output should be '1' otherwise output should be '0' and finally AND function has inverse behavior of OR function and this means that when both of inputs are '1', output should be '1' otherwise output should be '0'. The result from the operation depends on the first inputs and involves the implementation of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel. Resistance and capacitors are bad components to design a circuit (Ali Ghorbani, Mehdi Sarkhosh, Elnaz Fayyazi, Neda Mahmoudi and Peiman Keshavarzian, 2012), so for this reason we designed our circuit without these devices. Binary adders are one of the most important components in many modern digital circuits, especially processors. The parallel prefix adder employs the 3-stage structure of the CLA adder. The improvement is in the carry generation stage which is the most intensive one:

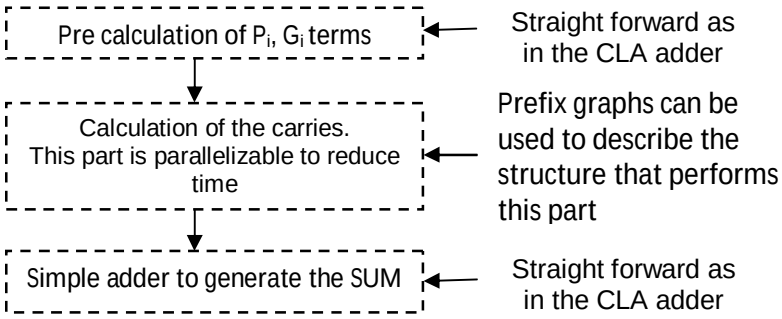


Fig. 1 . The 3-stage structure of the CLA adder

Table1: List of formula for implementation of a parallel prefix adder cell

$\forall \varepsilon$ Ai , Bi $\Longrightarrow$ Pi = Ai $\oplus$ Bi		$\forall \varepsilon$ Ai , Bi $\Longrightarrow$ Gi = Ai · Bi	
Mi	GSi	PMi	Ci
M1 = P0 · C0	GS1 = M3 + G2	PM1 = P1 · P2	C1 = M1 + G0
M2 = M1 · C1	GS2 = M5 + G4	PM2 = PM1 · C1	C2 = M2 + G1
M3 = P2 · G1	GS3 = M6 + G5	PM3 = P3 · P4	C3 = GS1 + PM2
M4 = P3 · C3	GS4 = M7 + G5	PM4 = PM3 · C3	C4 = M4 + G3
M5 = P4 · G3	GS5 = GS4 + PM7	PM5 = PM3 · P5	C5 = GS2 + PM4
M6 = P5 · GS2	$\sum_{i=0}^{7} Si = Ci \oplus Pi$	PM6 = PM5 · C3	C6 = GS3 + PM6
M7 = P6 · G5		PM7 = PM8 · GS2	C7 = GS5 + PM7
M8 = P7 · C7		PM8 = P5 · P6	C8 = M8 + G7
		PM10 = PM8 · PM3	

In proposed parallel prefix adder our delay and power consumption and delay product (PDP) are optimized than previous work. This design has been used 566 transistors based on CNTFETs, and compared their parameters with other prefix adders. $A_{(0-7)}$, $B_{(0\_7)}$ and C_0 are inputs and $S_{(0\_7)}$ and C_8 are outputs. Final design of the parallel prefix adder in gate level is shown in fig 2.

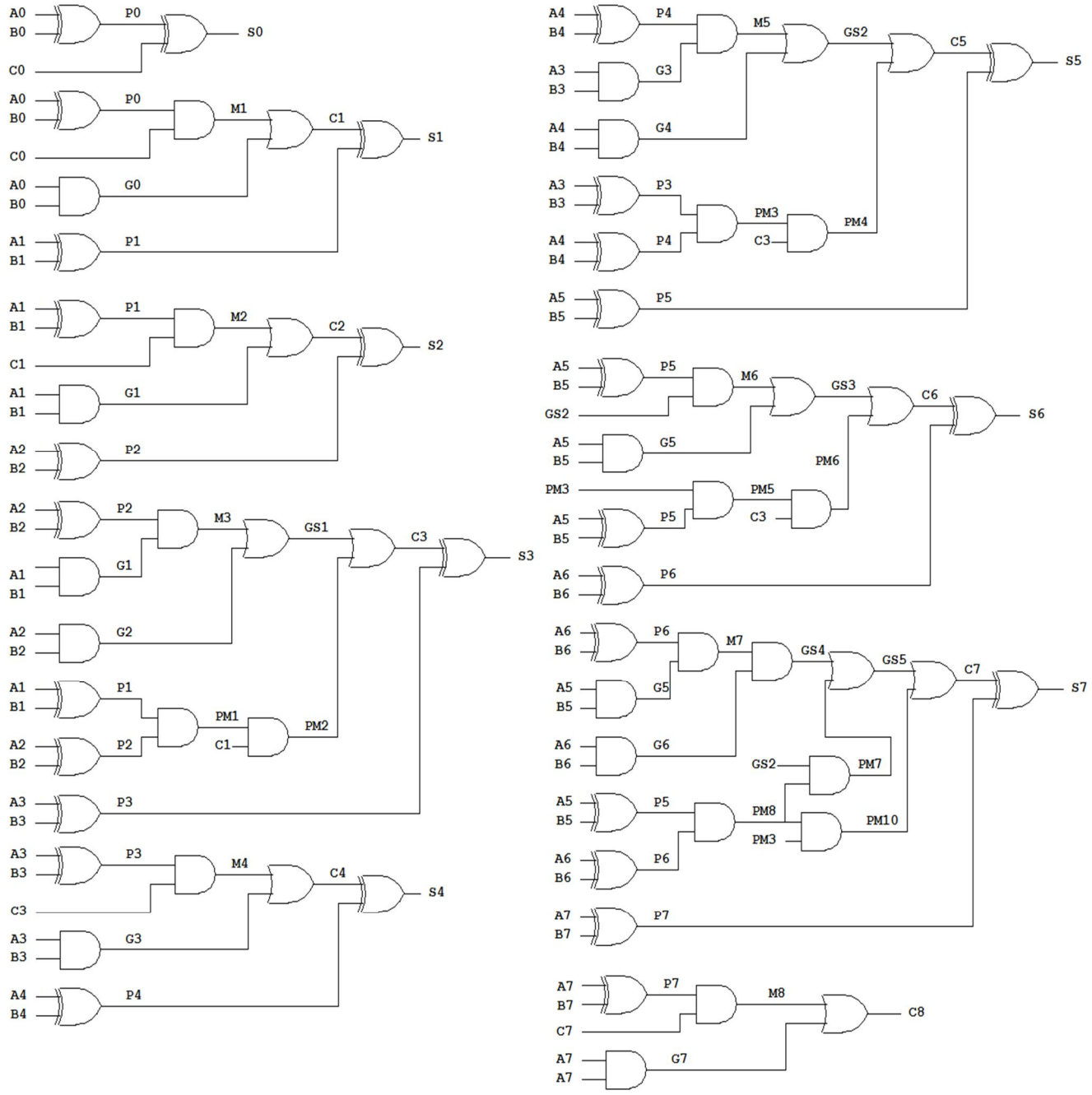


Fig .2 . Final design of parallel prefix adder in gate level

Internal structure apiece of OR/AND/XOR gates show in fig. 3, that for example A, B are inputs and XOR, AND, OR as outputs.

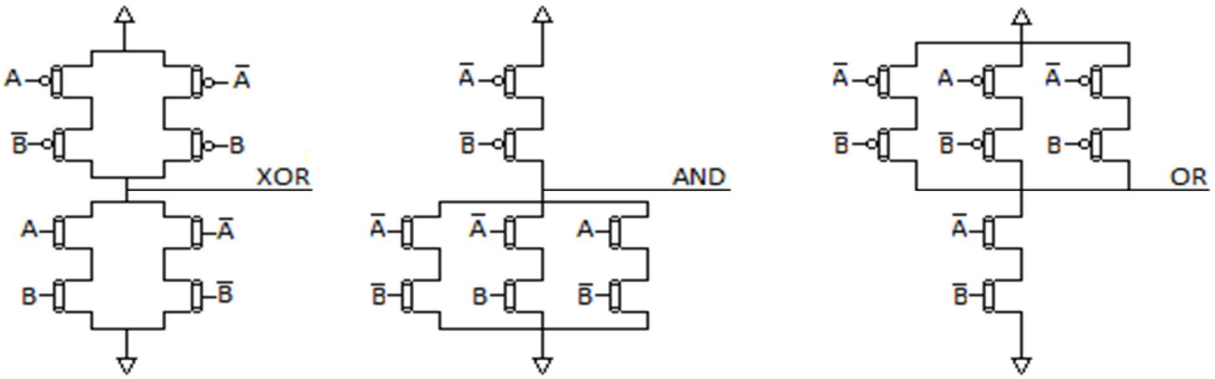


Fig. 3. Internal structure of gates

The following relationships are achieved from the output circuit:

S0: A0 ⊕ B0 = P0, P0 ⊕C0 = S0
S1: A0 ⊕ B0 = P0, P0 · C0 = M1, A0 ·B0 = G0, M1 + G0 = C1, A1 ⊕ B1 = P1, P1 ⊕ C1 = S1
S2: A1 ⊕ B1 = P1, P1 · C1 = M2, A1 ·B1 = G1, M2 + G1 = C2, A2 ⊕ B2 = P2, P2 ⊕ C2 = S2
S3: A2 ⊕ B2 = P2 , A1 · B1 = G1 , G1 ·P2 = M3 , A2 · B2 = G2 , M3 + G2 = GS1 , A1 ⊕ B1 = P1 ,A2 ⊕ B2 = P2 , P1 · P2 = PM1 , PM1 · C1 = PM2 , GS1 + PM2 = C3 , A3 ⊕ B3 = P3 ,P3 ⊕ C3 = S3
S4: A3 ⊕ B3 = P3, P3 · C3 = M4, A3 ·B3 = G3, M4 + G3 = C4, A4 ⊕ B4 = P4, P4 ⊕ C4 = S4
S5: A4 ⊕ B4 = P4 , A3 · B3 = G3 , G3 ·P4 = M5 , A4 · B4 = G4 , M5 + G4 = GS2 , A3 ⊕ B3 = P3 , A4 ⊕ B4 = P4 , P3 · P4 = PM3 , PM3 · C3 = PM4 , GS2 + PM4 = C5 , A5 ⊕ B5 = P5 ,P5 ⊕ C5 = S5
S6: A5 ⊕ B5 = P5, GS2 ·P5 = M6, A5 · B5 = G5, M6 + G5 = GS3, A5 ⊕ B5 = P5, PM3 · P5 = PM5, PM5 · C3 = PM6, GS3 + PM6 =C6, A6 ⊕ B6 = P6, P6 ⊕ C6 = S6
S7: A6 ⊕ B6 = P6 , A5 ·B5 = G5 , P6 · G5 = M7 , A6 · B6 = G6 , M7 · G6 = GS4 , A5 ⊕ B5 =P5 ,A6 ⊕ B6 =P6 , P5 · P6 =PM8 , GS2 · PM8 = PM7 , GS4 + PM7 = GS5 , PM3 · PM8 = PM10 ,GS5 + PM10 = C7 , A7 ⊕ B7 = P7 , P7 ⊕ C7 = S7
C8: A7 ⊕ B7 =P7, P7 · C7 = M8, A7 · B7 = G7, M8 · G7 = C8

The samples of outputs of this circuit are show in fig.4.

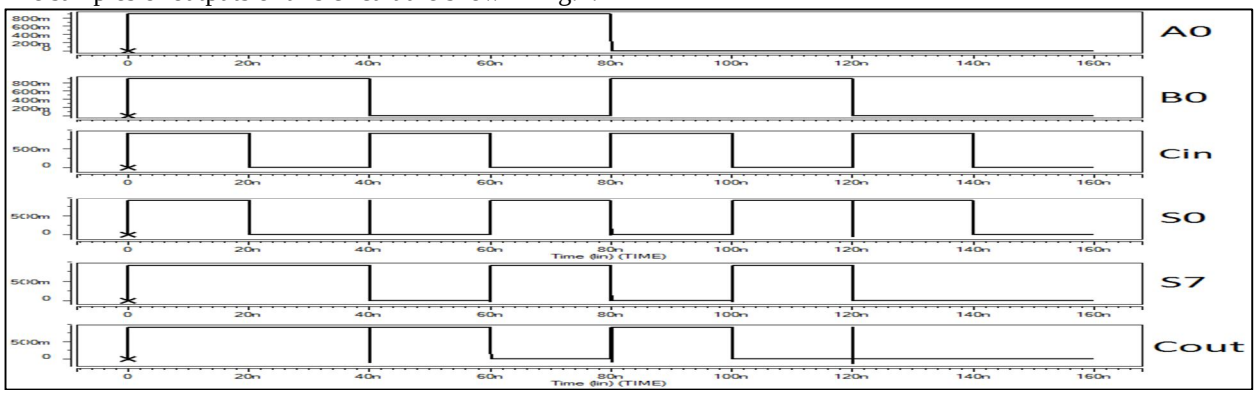


Fig. 4. simulation outputs

The output (PDP) of the circuit diagram at different temperatures and different voltages has drawn**.**

Table 2: simulation at different temperatures and voltages

V_{dd}\temperature	0° C	27° C	37° C	100° C
0.8 V	1.41904336e17	1.85856e17	2.25859926e17	2.734400062e17
0.9 V	1.8098336e17	2.45241456e17	2.9494528e17	3.46271536e17
1.0 V	2.19791386e17	2.9089151e17	3.6172976e17	4.72779846e17

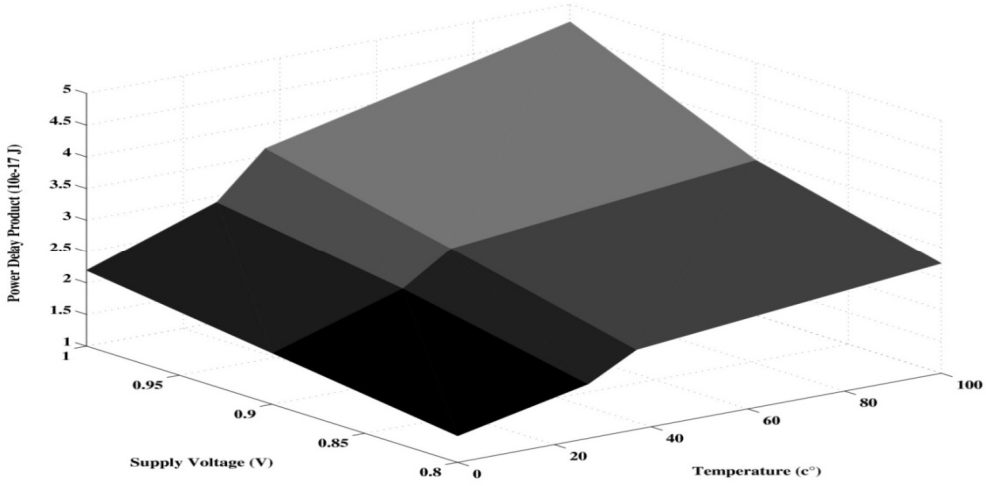


Fig.5. simulation outputs digram

5. SIMULATION RESULT

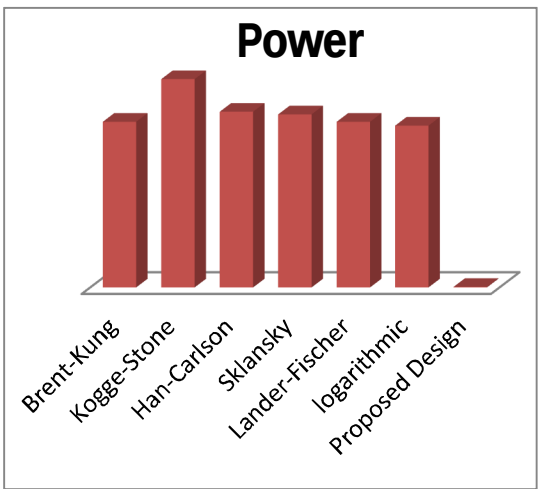
The HSPICE circuit simulator has been used to simulate the parallel prefix adder circuit. Simulation has been performed on the power consumption and power delay product (PDP). CNTFETs are simulated in 0.9v and delay is measured in worse case. When the inputs and outputs reach 50% of the supply voltage level the delay of our design is measured. The simulation results are shown in Table 3. To obtain average power and PDP we use below equations:

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{static} \quad (5)$$

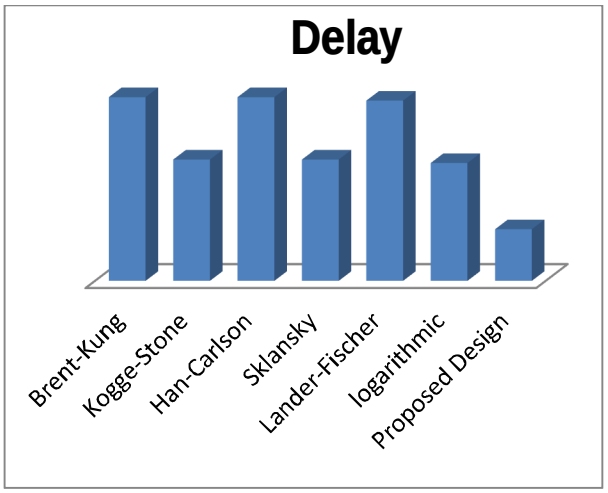
PDP = worse case Delay * Average power (6)

Table 3: simulation results

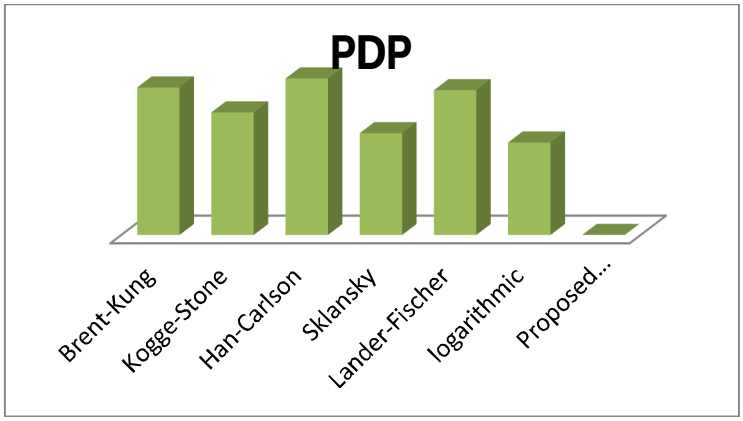
Designs	Power	Delay	PDP
Brent-Kung	49.76461E-6	0.53E-9	26.3752433E-15
Kogge-Stone	62.58961E-6	0.35E-9	21.9063635E-15
Han-Carlson	52.78991E-6	0.53E-9	27.9786523E-15
Sklansky	51.99499E-6	0.35E-9	18.1982465E-15
Lander-Fischer	49.76504E-6	0.52E-9	25.8778208E-15
Logarithmic	48.61100E-6	0.34E-9	16.52774E-15
Proposed Design	1.64680E-7	1.4892E-10	2.4524E-17



(a)



(b)



(c)

Fig. 6. Charts of simulation results

6. Conclusion

The parallel prefix adder was successfully designed and implemented in schematics and physical layout. The parallel prefix formulation of binary addition is a very convenient way to formally describe an entire family of parallel binary adders. Parallel prefix adder can be seen as a 3-stage process. Variations of parallel adders have been proposed. These variations are based on: Modifying the carrying generation equations and reformulating the prefix definition (Ling), Restructuring the carry calculation trees based by optimizing for a specific technology (Beaumond-Smith) and other optimizations. We proposed a design for prefix adder cells that used to reduce power consumption and power delay product (PDP) of circuits. In this paper for design a new prefix adder cells we used 566 transistors based on CNTFETs technology and used OR/AND/XOR gates for implementation this circuit. This circuit's transistors are simulated in 0.9v and beneficial HSPICE software. Simulation result shows that a new prefix adder cells can be achieved that their parameters improve more than previous work.

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