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A Novel Linear Low Voltage Rail to Rail Second Generation Current Conveyor for RF Applications

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ABSTRACT

In this paper, a novel second generation current conveyor (CCII) with simple structure in AB classification is presented. This offered circuit has rail to rail dynamic range in output and input terminals. Another specification of circuit is high capability to drive current at node z which can drive positive and negative output currents in AB classification mode. The CCII circuit was simulated in the standard 0.18µm CMOS TSMC technology with minimal count of CMOS transistors, simulation result is exhibited the parasitic resistance of 37ohm at node x. it is composed from negative and positive supply voltages ±0.75V with 750µw value of power consumption. The proposed circuit can be suitable for RF analog structures such as filters, oscillators and sigma-delta modulators because of the high frequency performance of current and voltage transfer functions. the -3dB cut-off frequency of proposed circuit for voltage and current transfer functions 3.87GHz and 3.23GHz was measured respectively. Rail to rail and high linearity performances of voltage transfer function and high linearity of dual positive and negative current transfer functions are other specification of suggested circuit.
KEYWORDS: current conveyor, current mode, low voltage, rail to rail, cut-off frequency.

INTRODUCTION

In the first time, the basic structure of second generation current conveyor (CCII) was expanded by Sedra and Smith [1]. Current conveyors can be applied in voltage and current analog components but the developed circuits of CCII are more applicable as one of the basic active elements in current mode analog interfaces such as filters, VCOs and data converters [2].

Recently, one of the state of the art subjects in consideration of analog current mode circuit researchers is development in performance parameters of CCII circuits. The results of these investigations lead to resolution increasing in current and voltage transfer functions, compensation of offset [3], improvement in transfer functions linearity[4] and high frequency features[5], optimization circuit toward low power and low voltage design [6] and trend for differential circuitry. Among these goals, the low power and low voltage circuit design and linearity range of CCII transfer functions are widely applicable in VLSI and current mode implementations moreover; high frequency performances of CCII can be applied greatly in mobile communication analog structures.

In this paper, the classical unity gain current conveyor is presented. The parameters of linearity boundary, frequency response and low voltage requirements have been improved in comparison other same works according to the simulation result. Moreover, the simple and differential structure of proposed CCII is another advantage of offered circuit. On the other hand, the circuit was implemented in class AB configuration and can be drive symmetric current in output nodes. For the flexibility sufficiency in implementation of analog current mode components has been used from double negative and positive output current nodes z^+ and z^-.

I. The Proposed CCII Circuit

Current conveyors are basic and applied active components in analogue interfaces and elementary signal processing cells. Basic construction of ideal CCII is formed by three ports, x, y and z. The model of CCII can be introduced negative or positive styles with regard to output current direction at node z. the direction of output current can be internal or external. Figure 1 shows the blocked style of positive implementation.

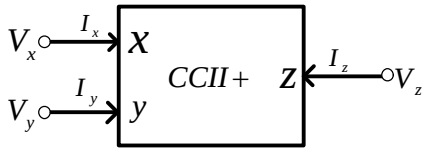

Figure 1: the block diagram scheme of the positive CCII

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The CCII can be explained by two sub-circuits: voltage followers and current-mirrors. Gains of current mirrors and voltage followers are one in the unity gain CCII. As a result, equations of unity gain type of CCII can be given by [7]:

$$V_x = V_y, I_y = 0, I_x = I_y \quad (1)$$

For realization of above equations, the circuit diagram of CCIIs can be assumed as arrangement of one differential transconductance and two single ones. They are located together in special configuration that that is shown in Figure 2. As is observed from Figure 2, the voltage follower circuit consists of two transconductances G1 and G2 that are located in negative feedback loop, the higher gain of negative feedback loop can cause to more accuracy in voltage transfer function and degradation of resistance in node x. In the figure 2, G2 and G3 construct the current mirror part. These must be equal for the unity gain accomplishment [8].

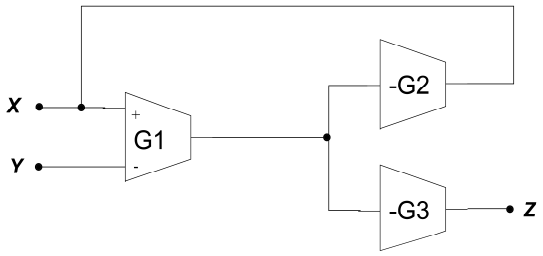

Figure 2: the scheme of location transconductances in CCII circuit

The offered circuit of CCII is shown in the figure 3. Its dimensions are optimized for high frequency and can be used in RF analog structures. The proposed circuit is implemented in the standard 0.18µm CMOS TSMC technology. Furthermore its configuration presents low voltage, rail to rail and high linearity features. Therefore dual differential pair of PMOS and NMOS transistors has been chosen for the input stage (M8, M9, M10 and M11) that can provide the rail to rail specification. As Figure 3 shows, transistors M8 and M11 prepare the input positive amplitude however the transistors M9 and M10 prepare the negative one. in this design active load of voltage follower stage is created by NMOS transistors (M14, M15) and PMOS transistors (M2, M4) as current mirrors as a result, the bias currents in dual lines of voltage follower stage are equal and consequently, is realized the same voltages in nodes x and y.

As shown in Figure 3,For equalization current at node x and current at node z^+ are used from current mirrors M5, M6, M16, M17 and for the same current with opposite direction at node z^- are used from current mirrors M18, M19, M20, M21, M22, M23.

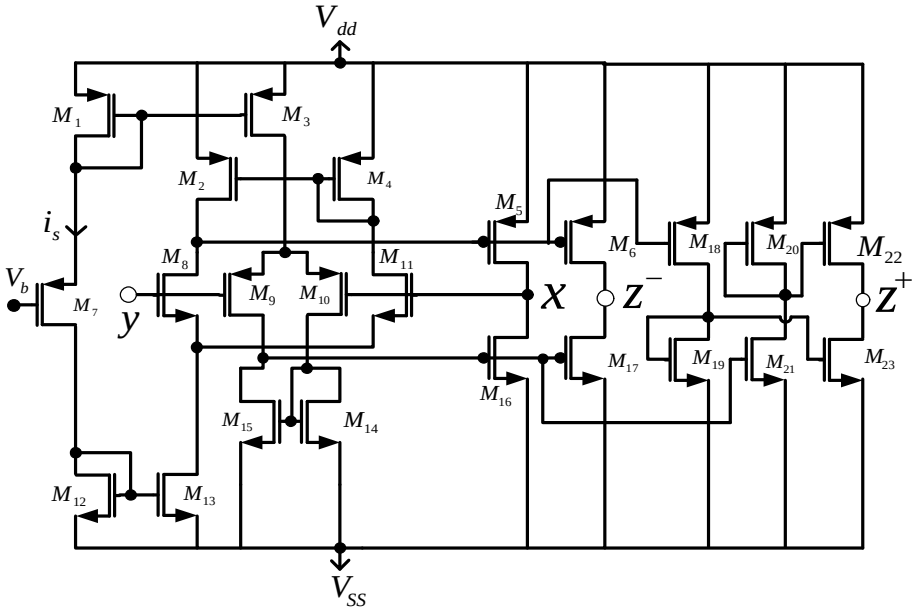

Figure 3: The schematic of suggested CCII circuit

As mentioned, the high loop gain of voltage follower circuit can be effective parameter for better accuracy of voltage transfer function and degradation of x node resistance, by a refer to Figure 3, the gain of transconductance G1,G2 and loop gain of voltage follower are given by following equations:

$$T_{G1} = g_{m8}(r_{d8} \| r_{d2}) + g_{m9}(r_{d9} \| r_{d3}) \quad (2)$$

$$T_{G2} = (g_{m5} + g_{m16})(r_{d5} \| r_{d16}) \quad (3)$$

$$T_{Loop} = T_{G1} \times T_{G2} \quad (4)$$

Where T_{G1} and T_{G2} are gain of transconductances according to Figure 2.

Moreover, the value of resistance at terminal x is approximately obtained by use of principles in negative feedback loop as follows:

$$R_x = \frac{r_{d5} \| r_{d16}}{T_{Loop}} \quad (5)$$

Where r_{d5} and r_{d16} are drain-source resistances M5 and M16. T_{Loop} can be situated from equation (4). Also as seen in output stage of figure 3, the output resistances at terminals z^+ and z^- can be characterized by following relations respectively:

$$R_{z^-} = r_{d6} \| r_{d17} \quad (6)$$

$$R_{z^+} = r_{d22} \| r_{d23} \quad (7)$$

In the above equations r_{d6}, r_{d17}, r_{d22} and r_{d23} are output resistances of M6, M17, M22, M23 respectively.

II. SIMULATION RESULT

The proposed low voltage and high frequency CCII is simulated in the standard 0.18µm CMOS TSMC technology. The HSPICE software has used for simulation and the used dimensions of CMOS transistors has been set in the table 1. The bias current of circuit (i_s) was measured of about $1\mu A$ in the standby condition. The suggested CCII is composed of dual symmetric supply voltages $\pm 0.75V$ that is indicated the low voltage characteristic. the overall power consumption of circuit is about $750\mu W$. Furthermore, V_b is set to -0.2V for the best performances and HSPICE simulation exhibited the parasitic resistance (R_x) 26Ohm at the terminal x. Figure 4 is shown variation of voltage at the port x versus the internal current of it. The slope of its linear carve have inverse ratio with R_x.

Figure 5 shows the linear relation between terminals x and y which identify the linearity specification of voltage transfer function. As shown in this figure, voltage in node x tracks the voltage in node y from -0.7Volt to +0.7Volt with linear curvature as a result, the rail to rail dynamic range of voltage variation can be employed.

Figure 6 shows the linear relation between internal and external output current of terminals z^+ and z^- versus the internal current of terminal x. these current transfer functions prove the capability of current drive in output stage of proposed CCII, because of the unity gain design, the voltage and current transfer function carves according to the Figures 5 and 6 have unit slope which their variation errors are less of 1%.

Table 1: the dimensions of CMOS transistor of proposed CCII

Transistors	W/L($\mu m / \mu m$)
M12	(0.5/0.18)
M14,M15	(1/0.18)
M1	(1.5/0.18)
M8,M11	(2/0.18)
M2,M4	(3/0.18)
M16,M17,M19,M21,M23	(4/0.18)
M9,M10	(6/0.18)
M5,M6,M18,M20,M22	(12/0.18)
M1	(24/0.18)
M7,M13	(30/0.18)
M3	(90/0.18)

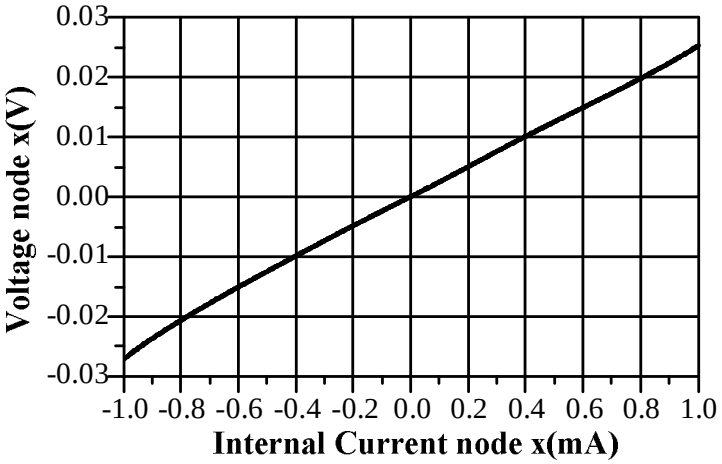

Figure 4: voltage at terminal x versus its internal current

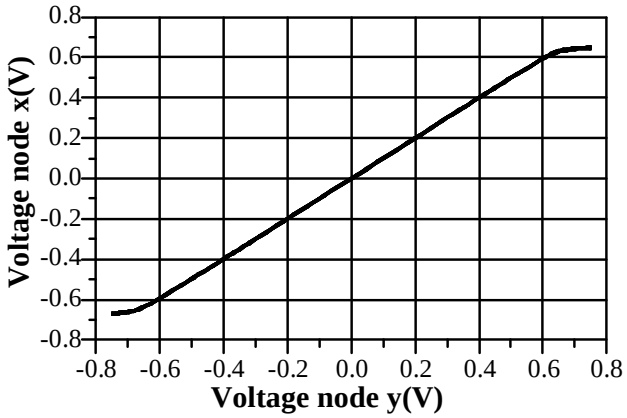

Figure 5: the voltage at node x versus the input voltage of node y

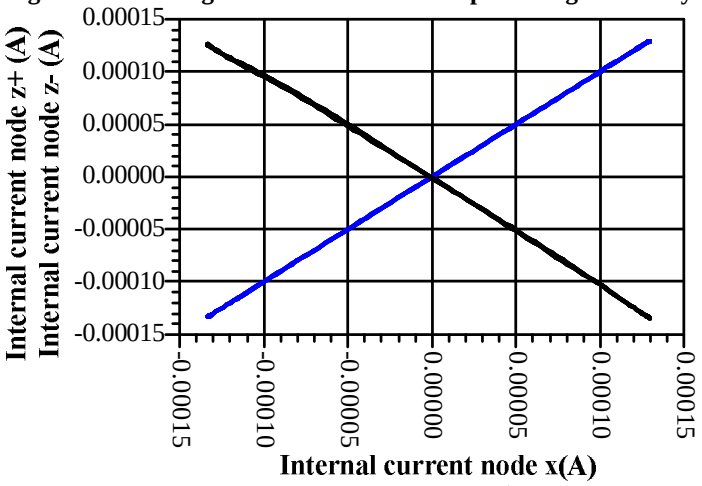

Figure 6: the output currents at terminals z^+ and z^- versus Internal current of terminal x

The figures 7 and 8 show the frequency response of voltage and current transfer functions. as seen, the -3dB cut-off frequencies for voltage and current transfer functions are 3.87GHz and 3.23GHz respectively, the specific of high frequency performances of proposed CCII can able it for using in analog RF components.

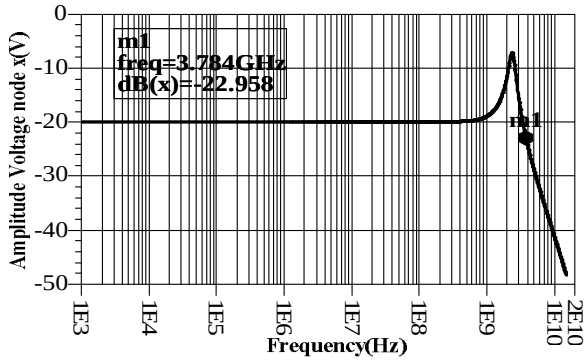

Figure 7: frequency response of voltage transfer function

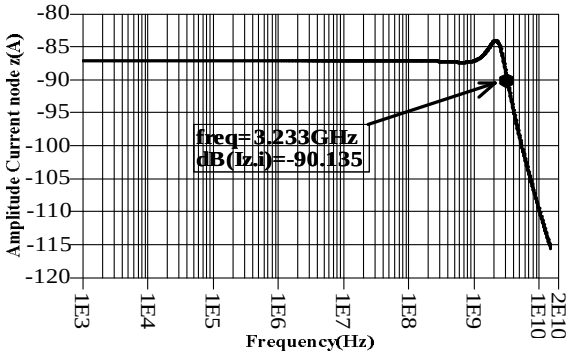

Figure 8: frequency response of current transfer function

III. CONCLUSION

In this paper, a class AB second generation current conveyor with CMOS transistors was designed and simulated. The proposed CCII have rail to rail linearity range in voltage and current transfer functions in comparison to other same works. The wide range bandwidth and low-voltage and low-power specifications were optimized. Furthermore, the proposed CCII has very low resistance at terminal x and it is capable to convert to other types by little changes in structure.

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