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A 0.5-V 17- µW Second-Order Delta-Sigma Modulator Based on a Self-Biased Digital Inverter in 0.13µm CMOS

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ABSTRACT

This paper proposes a self-biased digital inverter circuit and its application in a low power 2nd order switched-capacitor delta-sigma modulator. By employing the self-biasing technique, the gain performance of the modulator is improved and increased the power efficiency. The modulator is designed by using standard CMOS 0.13µm technology. The threshold voltages of the PMOS and NMOS transistors are 320mv and 380mv, respectively. All transistors are operated within the supply voltage 0.5 V. The designed modulator achieves 63.6dB Signal-to-noise ratio (SNR) and 63.6dB Signal-to-noise and distortion ratio (SNDR) in an input signal bandwidth of 8 KHz with a sampling frequency of 1.6 MHz. The modulator core consumes only 4µW of power and the total power consumption is 17µW. The proposed delta-sigma modulator achieves high power efficiency, low power, low voltage and high speed performances for practical applications.
KEY WORDS: Delta-Sigma Modulator. Self-Biased Digital Inverter. Low-Power. Low-Voltage.

1. INTRODUCTION

The continuing CMOS technology scaling has enabled the digital systems by using a proportional reduction of the supply voltage to maintain the device's reliability and also decrease power consumption and lower costs. Therefore, the design of low power, low voltage and high speed analog circuits is always faced with challenges. In order to overcome these challenges several techniques have been investigated in many papers [1]-[8]. To design low voltage analog circuits, they use charge pumps [1], [2] switched-op amps [3], switched-RC [4] and the input-feed forward architecture [5]. A charge pumps technique generates higher voltage than the supply voltage for switches [1], [2]. To eliminate the need for charge pumps, switched-op amps technique with common mode level shift has been reported in [3]. Since switched-op amps circuits face a tradeoff between speed and accuracy, switched-RC technique which achieves high linearity and low-voltage operation are used in [4]. All above mentioned techniques may require extra control circuits and extra current which consumes more power and occupy the large area. To minimize the power consumption in a low-voltage environment, ultra-deep-submicron standard digital CMOS technologies are investigated [5] and also the input feed-forward architecture with the low-power operational transconductance amplifier (OTA) is proposed [6]. The supply voltages of the OTAs are confined and have reached the limits of further scaling, because they are strictly limited by the input common-mode voltage and they have complex circuitry to implement. Thus, to remove the need for OTAs, inverter-based amplifiers and self-biased fully differential super inverter has been reported recently [7], [8]. The most important reason using an inverter instead of amplifiers is simplicity and the capability of operating with ultra-low supply voltages [7]. The single-ended inverter utilized instead of an OTA in delta-sigma modulator is replaced by the self-biased fully differential super inverter to increase its noise rejection which complicates the common-mode feedback design [8]. To improve the inverter's gain performance and attain higher power efficiency, low voltage, high speed and especially low power a self-biased digital inverter is presented and analyzed in this paper. By employing the self-biasing technique, the digital inverter enables circuit to be less sensitive to process, supply voltage and temperature (PVT) and parameter variations. In this case, the switching currents can be greater than the quiescent bias current. Also the external biasing voltages become unnecessary in this structure, thus saving power and die area. Therefore, the proposed self-biased digital inverter is suitable to use in switched-capacitor circuits for low power, low voltage and high speed. As a prototype, a low power second-order, single bit delta-sigma modulator based on a self-biased digital inverter is designed for practical applications. This paper is organized in the following manner. Section 2 describes the operation principle of a self-biased digital inverter. Section 3 discusses the details of the architectural delta-sigma modulator. Section 4 has simulation results, and section 5 provides conclusions.

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2. SELF-BIASED DIGITAL INVERTER

Instead of using self-biased super inverter structure that has been reported in [8], a self-biased digital inverter is proposed as illustrated in Fig.1. Compared to self-biased super inverter structure, the self-biased digital inverter structure not only achieves excellent power efficiency but also is compatible with very low voltage. Moreover, in this structure supplying switching currents can be much greater than the quiescent bias current which is one of the advantages for high speed and low power applications. One important design aspect in this structure is the size of transistor and the region of biasing. Thus, the transistors used in main inverter and biasing inverter should be biased in linear region and are equally sized. In order to have a circuit that can be compensate any PVT variation during circuit operation and stabilized the bias voltages, M_1 and M_2 are used in the negative feedback loop. In this case, transistors M_1 and M_2 are biased in linear region. Therefore, the V_H and V_L can be set very close to supply voltages. In fact, these two voltages determine the output swing which can be very close to difference between the two supply rails [9], [10]. The differential-mode gain (A_{dm}) of the self-biased digital inverter is given by:

$$A_{dm} \cong \frac{g_{m1} + g_{m2}}{g_{out}} \qquad (1)$$

Where g_{m1} and g_{m2} are the transconductances of transistors $M_{pm\text{-}pb}$ and $M_{nm\text{-}nb}$, respectively and g_{out} is the output conductance of the self-biased digital inverter.

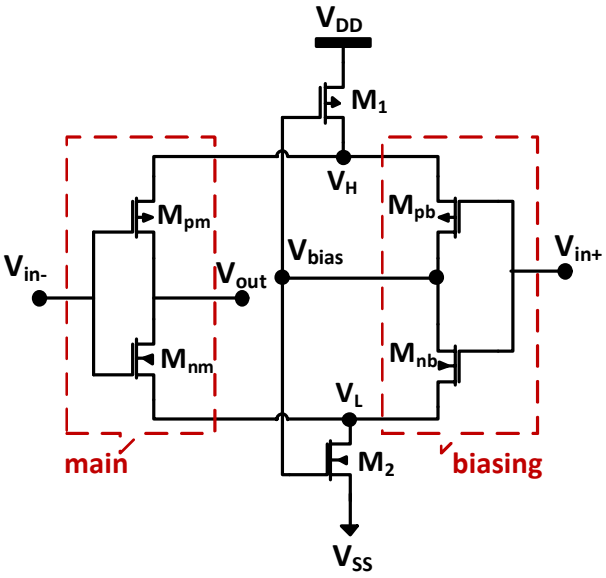


Fig.1. Circuit schematic of self-biased digital inverter

3. COMPLETE DELTA-SIGMA MODULATOR CIRCUIT

To design delta-sigma modulator circuit, several important criterions should be considered. The order of a modulator demonstrates the number of integrators. The choice between single loop and cascade architecture is a criterion should be noted. The choice between a single bit and multi bit quantizer that prepares B bits of resolution. The oversampling ratio is determined as the ratio of the modulator sampling rate to its Nyquist rate. The complete non cascaded 2nd order delta-sigma modulator circuit is shown in Fig.2. In this structure single loop architecture with a negative feedback, two integrators and a 1-bit quantizer is utilized. The self-biased digital inverter is used instead of externally-biased operational amplifiers in the switched-capacitor integrators for low-voltage low-power applications. To have high linearity performance a single bit quantizer is applied in the modulator. Since the key element in a delta-sigma modulator is the integrator, a switched-capacitor integrator incorporating the self-biased digital inverter operates with two phase clocks, sampling (Φ_1 & Φ_{1s}) and integration (Φ_2 & Φ_{2i}) phases, as illustrated in Fig.3. In the differential-mode operation, the input signal is sampled in the sampling capacitors (C_s) during the sampling phase. In order to eliminate signal dependent charge injection, the Φ_1 is turning off slightly earlier than Φ_{1s}. During integration phase, Φ_{2i} is turning on slightly earlier than Φ_2 to shift the floating potential to common-mode voltage level. As soon as, Φ_2 switch is closed, the differential charges in sampling capacitors (C_s) are transferred to the feedback capacitors (C_f). Figure 4 shows the timing diagram of the non-overlapping clocks. All switches are NMOS only transistors and the input voltage amplitude of the clock generator is set to 0.7 V to ensure an adequately low switch resistance in a low supply voltage. The used sampling capacitors C_s in this integrator are completely matched and the capacitors values in this circuit are chosen as 100 pF. If the sampling capacitors values are less than 100 pF, the output voltage noise at the switched-capacitor integrator will be increased. In this structure, two anti-parallel PMOS transistors are

connected in a negative feedback between the input and output ports of the self-biased digital inverter. These two PMOS transistors are equivalent two very large pseudo-resistors which balance the two common-mode voltages. Therefore, the differential gain does not decrease and occupy a smaller area than the resistor [8].

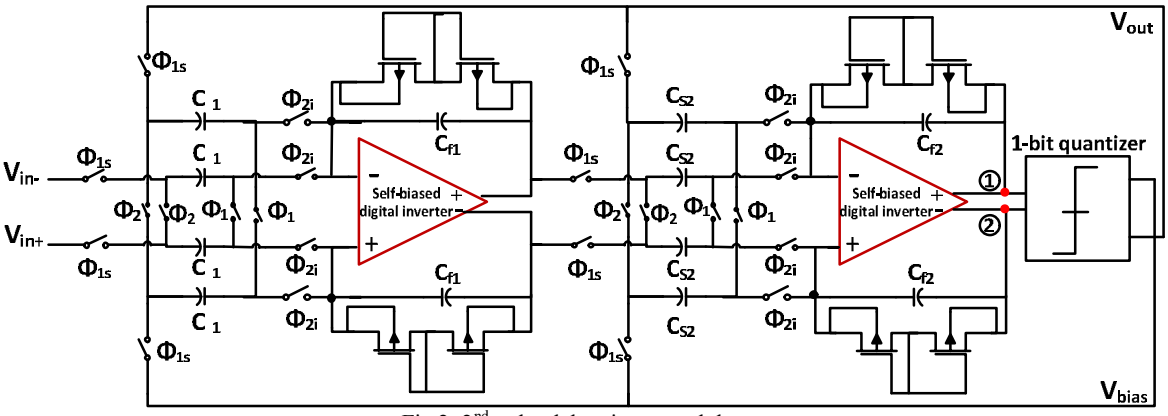


Fig.2. 2nd order delta-sigma modulator

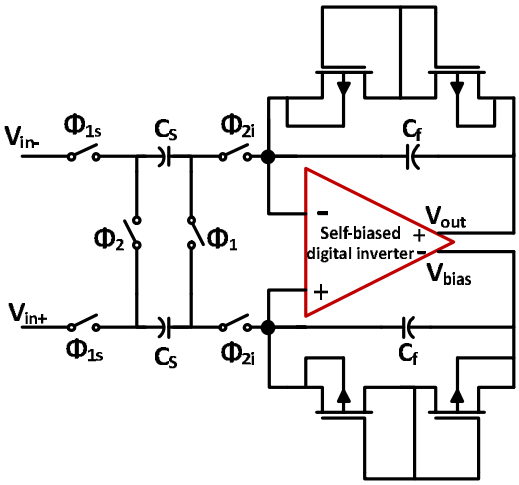


Fig.3. A switched-capacitor integrator incorporating the self-biased digital inverter

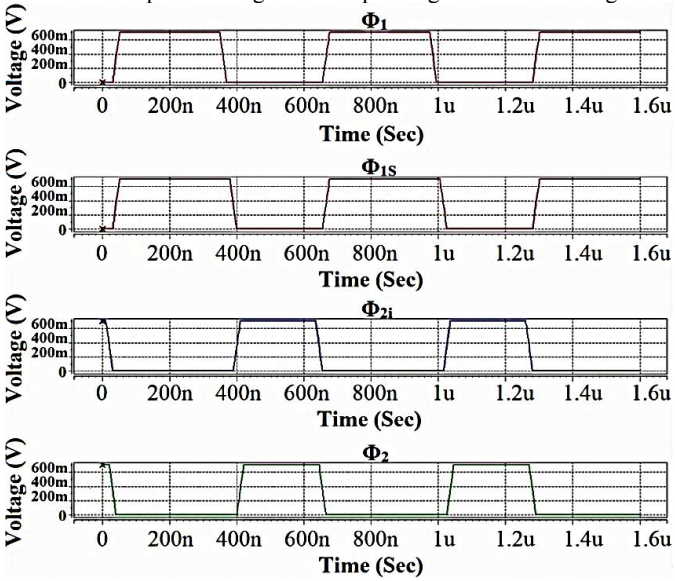


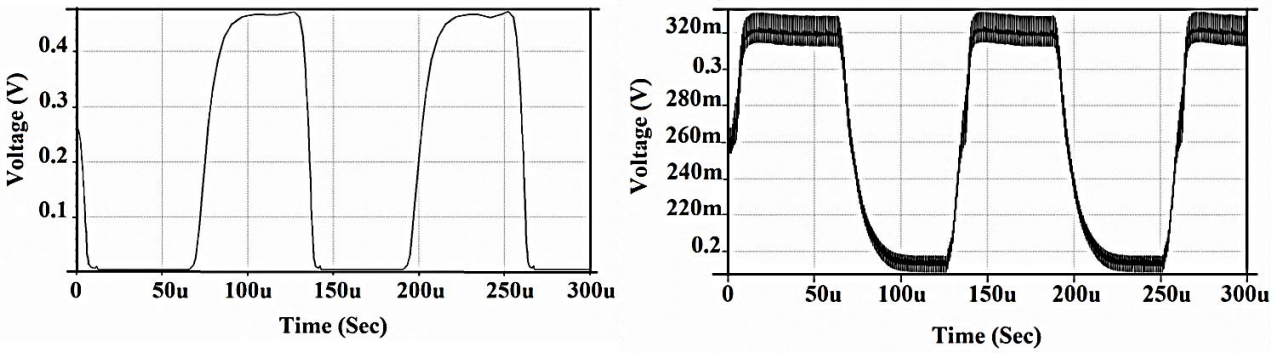
Fig.4. Timing diagram

4. SIMULATION RESULTS

The proposed delta-sigma modulator is implemented in a 0.13µm CMOS technology. The design specifications of the modulator are summarized in Table 1. The simulated voltage waveforms at the output of the delta-sigma modulator (node 1 and node 2 in Fig.2.) for V_{dd}=0.5 V are shown in Fig.5 (a), (b). Figure 6 shows the measured SNR for V_{in}=1$V_{P\text{-}P.diff}$ versus supply voltage. The measured SNR and SNDR are 63.6dB and 63.6dB, respectively for an 8 KHz bandwidth with a 0.5 V supply voltage. Compared to a 2nd order delta-sigma modulator incorporating the self-biased super inverter which consumes 4.8µw of power in the core [8], the power consumption in the core of the proposed 2nd order delta-sigma modulator in this paper is only 4µW and the total power consumption including the clock generators is 17µW. The measurement of results at both 0.5 V and 1V power supplies are summarized in Table 2. The performance of our delta-sigma modulator is compared with other switched-capacitor delta-sigma modulators in Table 3. To compare the performances, the common figure-of-merit (FOM) equation [7] is utilized as follows:

$$FOM = \frac{Power}{2^{(SNDR[dB]-1.76)/6.02} \times 2 \times BW} \qquad (2)$$

Due to use a self-biased digital inverter, the presented modulator operates at the lowest voltage while maintaining an excellent FOM. Also, this modulator achieves an excellent performance in the power efficiency.



(a) (b)

Fig.5. Simulated voltage waveforms at the output of the delta-sigma modulator for V_{dd}=0.5 V: (a) Node 1 in Fig.2. (b) Node 2 in Fig.2.

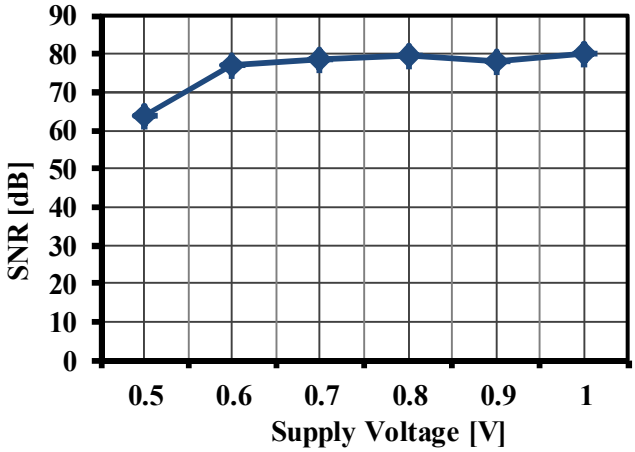


Fig.6. SNR for V_{in}=1 $V_{P\text{-}P.diff}$ versus supply voltage

Table 1. Design specifications of the modulator

Technology (V_{TN},V_{TP})	0.13µm CMOS (380mV, 320mV)	
Sampling Frequency	1.6 MHz	
Input Bandwidth	8KHz	
Sampling Capacitors (pF)	C_{S1}=100	C_{S2}=100
Feedback Capacitors (pF)	C_{f1}=0.8	C_{f2}=0.6

Table 2. Summary of simulation results

Supply Voltage	0.5 V	1 V
Peak SNR @8KHZ	63.6 dB	80 dB
Peak SNDR @8KHZ	63.6 dB	80 dB
Power Consumption in the core	4 µW	29.8mW
Total Power consumption	17µW	230mW
FOM (pJ/Conversion step)	0.202	230

Table 3. Performance comparison of delta-sigma modulators

Reference	Process (µm)	BW (KHz)	V_{dd} (V)	power (µW)	SNR (dB)	FOM (pJ/step)
[1]	0.35	25	1	950	87	1.31
[3]	0.18	8	0.7	80	70 @ 2KHz	2.7
[4]	0.35	24	0.6	1000	77	3.6
[5]	0.09	20	1	140	85	0.38
[6]	0.13	20	0.9	60	82.2	0.406
[7]*	0.35	8	1.2	5.6	72	0.303
[8]	0.13	8	1.2	4.8	67 @ 2KHz	0.58
This work	0.13	8	0.5	4	63.6	0.202

* Modulator-II in [7] is used for comparison

5. CONCLUSION

A 0.5-V 17-µw second-order delta-sigma modulator based on a self-biased digital inverter is realized in this paper. The prototype second-order delta-sigma modulator employing the self-biasing technique has been designed in 0.13µm CMOS technology using only standard V_{TH} devices and consumes only 4µW of power in the core. The presented modulator achieves a peak SNR of 63.6dB over a signal bandwidth of 8 kHz with a sampling frequency of 1.6 MHz. The simulation results show that this modulator can be used for very low voltage and low power practical applications.

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