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Design of an LNA in 0.18 µm CMOS Technology with a Flat and High Gain Covering Full Ultrawideband for Low Power Applications

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ABSTRACT

In this paper an ultrawideband low noise amplifier is proposed. The structure is based on 0.18 µm CMOS technology. The design is based on the current reusing structure to provide the wide band characteristics. A wideband flat gain (S21) about 20dB is achieved, stability of the structure over the whole desired frequency range is provided. Due to careful selection of the elements and biasing conditions, total power consumption of the topology from a 1.8 v supply is 3.4 mw. Another specific characteristic of the design is the comparatively low noise figure, less than 1.7 dB over the whole band of frequency.
KEY WORDS: Low Noise Amplifier, Low Power, High and flat gain, Ultrawideband.

1 INTRODUCTION

Ultrawideband communications capable of transmitting data over a wide range of frequency has been greatly growing in recent years. Great potential of utilization in consumer electronics applications like image and surveillance systems, wireless systems for both home and business applications and ground penetrating radars are the specifications of this technology which has attracted enormous attention. On the other hand the increasing demands for portable wireless systems especially wireless transmission in short range such as PCs, cellular phones, digital cameras and PDAs has caused the development of CMOS Radio Frequency Integrated Circuits (RFIC). The application of Wireless communications is mainly in wireless personal networks (WPAN), Medical image systems and vehicular communications [1].

The frequency range dedicated to ultrawideband systems by Federal Communication Commission (FCC) is approved to be from 3.1 to 10.6 GHz, which is 7500 MHz of the frequency band. High data rate transmission in addition to low power consumption, low cost and high security can be mentioned as the characteristics of this standard.

Low noise amplifier as the first block of the receiver wireless systems should add a very low noise while it amplifies the received signal from the antenna to a desirable level over a relatively broad range of frequency. Gain flattening in the full bandwidth, providing good impedance matching and a low noise figure are also expected from a practical LNA.

One main concern in designing an LNA is providing a balance between the design parameters like gain, noise, matching, stability and linearity in order to optimize the radio frequency system.

Lowering the power consumption is also expected in the LNA design so that the design integration would not be problematic.

Obviously a variety of research has been done in designing an efficient topology in recent years, but when it comes to implementation and fabrication one main unsolved problem is the large power dissipation of these structures [2].

For the purpose of reducing the power consumption some topologies are previously introduced; In order to qualify CG and CS structures in this regard some comparisons are made which in this case CS is proved to be more efficient [3]. Power consumption in current reusing structures in which there's just one path of current flow is greatly lowered [4]. Stagger tuning technique has been presented for low power UWB LNAs [5]. An ultrawideband LNA by utilizing gm-boosting technique and a modified form of noise canceling technique is also presented previously [6]. Peaking techniques are also proved to be useful in this regard [2,7]. Resistive-feedback inverter is employed to achieve wideband input matching [8]. An LNA using moderately inverted MOSFETs is also designed to achieve low power dissipation [9].

All these topologies face serious problems and suffer some deficiencies like not being able to provide a gain, high enough to meet the needs of the topology or flat and wide enough to cover the whole band or having a very high noise that makes the system inefficient or even the high power consumption is troublesome.

An ultrawideband LNA with higher gain which also has better noise performance and lower power consumption is presented in this paper. The structure is implemented by utilizing current reusing technique. Although using on chip inductors is not very desirable because of the large area they consume on the chip, the performance they provide in comparison to their inductorless counterparts makes their usage unavoidable. The stability and linearity of the structure are also well provided.

In the following parts, first the proposed structure is elaborated and explained in part 2. In part 3 the equivalent circuit model is presented and the gain and resonant frequencies are formulated for further discussions on the design. In part 4 the simulation results are observed and then the results are discussed and compared with other previous works. The conclusion is finally presented in part 5.

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2 PROPOSED LNA DESIGN

The proposed LNA structure is demonstrated in Fig. 1. The first stage is a common source amplifier (M_1) and the common gate amplifier (M_1) is the second stage. These two stages take advantage of the current reusing technique by forming a cascode structure. Its application is the good amplification it provides for the received signals from the antenna, so that the desirable gain is achieved. The first stage also takes part in input impedance matching of the structure. Input matching network is realized by C_1, L_1 and L_2. R_1 provides a negative feedback and a bias path to the gate of M_1. R_2 is added to bias the circuit and limit the current flow down to the circuit, inorder to lower the power consumption.

The finall stage is a buffer following the cascode one. It is a combination of a source follower amplifier (M_3) and a current source (M_4). C_2 provide output matching. The mutual coupling of L_4, L_5 is expressed by k-factor which is defined as M/L, where M is the mtual inductance and L is the inductance of each inductor. So K represents the mutual inductance between L_4, L_5. The T-coil structure in output of the cascode structure is added to achieve wideband output response [2].

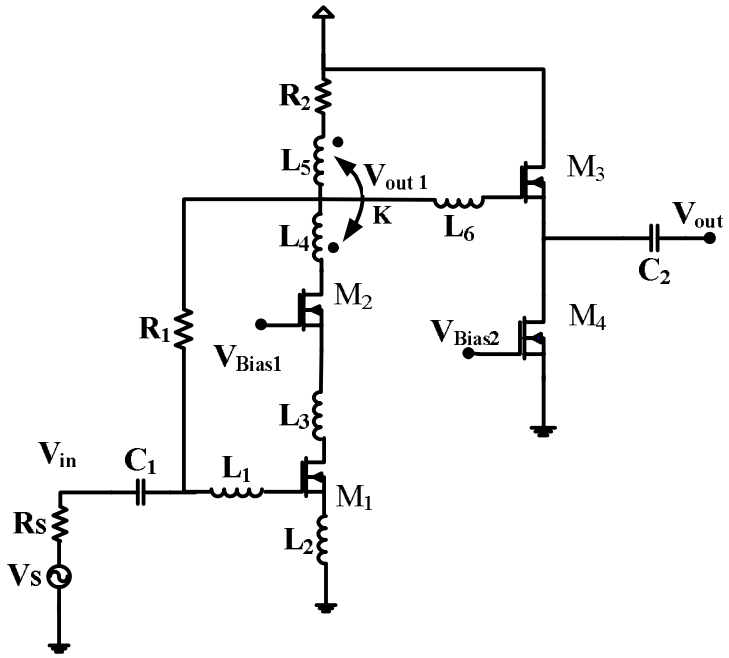

Fig.1. The proposed UWB LNA schematic.

The previlage of cascode structure over cascade one is that there is just one path of current needed in the former which greatly lowers the power consumption. The simulation results demonstrate that the power saving efficiency is about 24% in the current reusing structure [4]. The passive elements placed in the first inter-stage, have specified advantages. First they provide one same current path without extra power consumption. Second they can bring out a resonant frequency along with the parasitic elements of the transistors around them, so that they can compensate the gain roll off in the middle band. The resonant frequency in the low-band is named f_L. The second inter-stage between M_2 and M_3 provide high-band resonant frequency f_H . The combination of these two frequencies provide a flat gain and eventually ultrawideband structure. This technique is called stagger tuning and provides full-band structure [4]. The stagger tuning technique is illustrated in Fig.2.

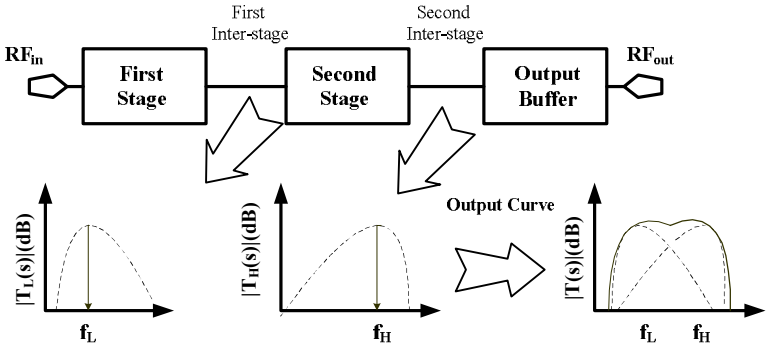

Fig.2. Stagger tuning technique.

3 DESIGN FORMULATION

3.1 Gain Formulation

The advantage of gain formulation is the good view point it provides about the effect of each element on gain in order to be able to design the structure in a way that it has the best efficiency. In other words when the application of each element

is well understood, the elements can be designed for the structure's best performance. Figure 3 demonstrates the equivalent circuit model of the cascode stage. The formulation is done step by step for each stage shown on Fig. 3.

$$L_M = L_4 + M \quad , \quad L_N = L_5 + M \qquad L_P = -M \tag{1}$$

M is the mutual inductance between L_4 and L_5 .

Z_1 is specified as equivalent impedances found at the output on Fig. 3 and is defined as:

$$Z_1 = (sL_N + R_2) \| (\frac{R_1 A'_V}{1 - A'_V}) \| sL_P \| Z' \tag{2}$$

Z' is the loading effect of the next stage and is large enough to be ignored while calculating the impedance Z_1, and A'_V is $\frac{V_{out1}}{V_5}$ as shown on the equivalent circuit of Fig.3. It should be considered that the values of the elements are carefully chosen so that sLp has the smallest impedance among the parallel elements in Z_1. So Z_1 can be approximately taken equivalent to sLp.

$$Z_1 = sLp \tag{3}$$

The steps of voltage gain calculation are presented in the following equations.

$$\frac{V_{out1}}{V_1} = \frac{Z_1}{Z_1 + sL_M} = \frac{L_p}{L_P + L_M} \tag{4}$$

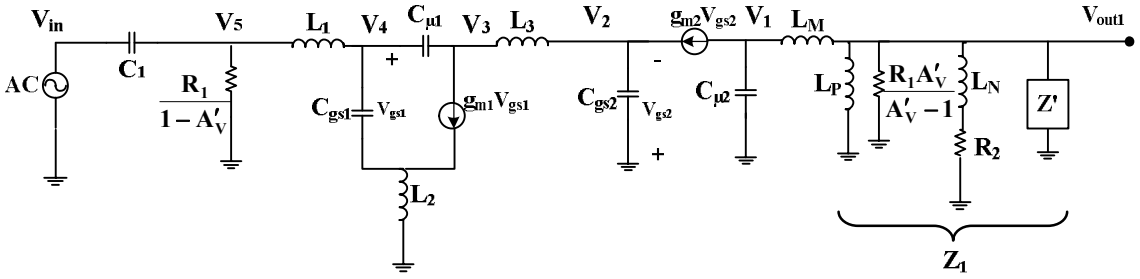

Fig.3. The equivalent circuit model of the cascode stage of the proposed UWB LNA.

For calculating second gain stage:

$$\frac{V_1}{V_2} = \frac{g_{m2} s(L_P + L_M)}{s^2 C_{\mu 2}(L_P + L_M) + 1} \tag{5}$$

For the next stage:

$$\frac{V_2}{V_3} = \frac{1}{s^2 L_3 C_{gs2} + s g_{m2} L_3 + 1} \tag{6}$$

The same will be done for the next two stages:

$$\frac{V_3}{V_4} = \frac{N_1(s)}{D_1(s)} \tag{7}$$

In which:

$$N_1(s) = s^5 C_{gs2} C_{\mu 1} C_{gs1} L_2 L_3 + s^4 \{C_{gs2} L_3 L_2 g_{m1} C_{\mu 1} + g_{m2} L_2 L_3 C_{\mu 1} C_{gs1}\} + s^3 \{C_{gs2} C_{\mu_1} L_3 + g_{m2} g_{m1} L_2 L_3 C_{\mu 1} + C_{gs1} C_{\mu 1} L_2\} + s^2 \{L_2 C_{\mu 1} g_{m1} + g_{m2} C_{\mu 1} L_3\} + s\{C_{\mu 1} - g_{m1} g_{m2} L_3\} - g_{m1} \tag{8}$$

$$D_1(s) = s^5 C_{gs2} C_{\mu 1} C_{gs1} L_2 L_3 + s^3 \{C_{\mu 1} L_2 L_3 (C_{gs1} g_{m2} + C_{gs2} g_{m1}\} + s^2 \{g_{m2} C_{\mu 1} L_3 + L_2 g_{m1} (C_{gs2} + C_{\mu 1}) + C_{gs1} L_2 g_{m2}\} + s\{C_{\mu 1} + C_{gs2} + g_{m2} g_{m1} L_2\} + g_{m2} \tag{9}$$

For the next stage:

$$\frac{V_4}{V_5} = \frac{s^2 L_2 C_{gs1} + s L_2 g_{m1} + 1}{s^2 C_{gs1}(L_2 + L_1) + s L_2 g_{m1} + 1} \tag{10}$$

And finally:

$$\frac{V_5}{V_{in}} = \frac{sC_1 R_1}{A'_V + sR_1 C_1} \tag{11}$$

Because of the careful choice of the elements' values, the highest order term in (8) and (9) are dominant so that the relation (7) can be approximately equal to 1.

The constant term in (10) is also the dominant one for the reason of elements' values selection in high frequency for both nominator and denominator, so again this relation is approximately equal to 1.
The final gain relation is determined using relations (4) to (11) and after some calculations and simplifications it is as:

$$A_V = \frac{V_{out1}}{V_{in}} = A'_V \times \frac{sC_1R_1}{A'_V + sC_1R_1} \tag{12}$$

And A'_V can be consequently determined as:

$$A'_V = \frac{V_{out1}}{V_5} = \frac{L_P}{L_P + L_M} \times \frac{sg_{m2}(L_P + L_M)}{s^2C_{\mu 2}(L_P + L_M) + 1} \times \frac{1}{s^2L_3C_{gs2} + sL_3g_{m2} + 1} \tag{13}$$

It is obviously proved that voltage gain and consequently S21 is increased by increasing R_1 and L_P and g_{m2} and decreased by increasing L_3. This result for L_3 is verified by taking advantage of the simulation used in Fig. 4.

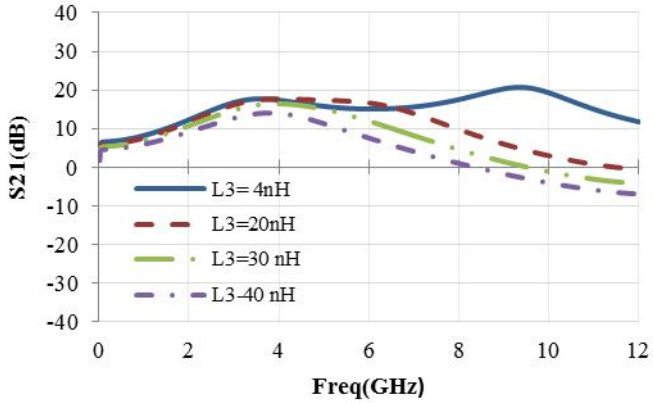

Fig.4. The effect of changing L_3 on gain

3.2 Resonance Frequency Formulation

In order to formulate the resonant frequencies, first the equivalent circuit models of the inter-stages are provided and then the impedance of the inter-stage is calculated. By setting the real parts of the denominator of the inter-stage impedance the resonant frequency is achieved.
The first inter-stage can be modeled as Fig. 5.

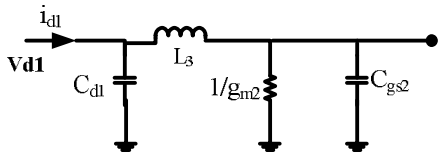

Fig.5. The first inter-stage equivalent circuit.

C_{d1} is the equivalent capacitance observed from the drain of M_1. To determine the f_L, the low-band resonant frequency, the impedance of first inter-stage should be considered according to the equivalent model of first inter-stage as:

$$Z_{TL} = \{(\frac{1}{sC_{gs2}} \| \frac{1}{g_{m2}}) + sL_3\} \| \frac{1}{sC_{d1}} \tag{14}$$

The denominator of Z_{TL} can be expressed as:

$$D(s) = s^3L_3C_{d1}C_{gs2} + s^2L_3C_{d1}g_{m2} + s(C_{d1} + C_{gs2}) + g_{m2} \tag{15}$$

So the low-band resonant frequency can be determined as:

$$f_L = \frac{1}{2\pi}\sqrt{\frac{1}{L_3C_{d1}}} \tag{16}$$

According to the values that are chosen for the elements this result can be confirmed by simulation results in which the low band resonant frequency is about 2GHz.
The second inter-stage can be modeled as in Fig. 6.

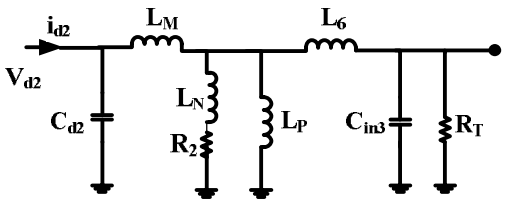

Fig.6. The second inter-stage equivalent circuit.

The impedance of this inter-stage can be determined as follows:

$$Z_{TH} = \{[\{(R_T \parallel \frac{1}{sC_{in3}}) + sL_6\} \parallel (sL_P \parallel (sL_N + R_2))] + sL_M\} \parallel \frac{1}{sC_{d2}} \quad (17)$$

Where R_T is the total resistance of the L_N along with the R_{ds2}. C_{in3} is the internal capacitances of M_3.
The denominator of Z_{TH} is calculated as in the following relation:

$$D_H(s) = s^5(L_P L_6 L_N R_1 C_{in3} C_{d2}) + s^4(L_M L_6 C_{in3}(L_P + L_N) + L_P L_N L_M R_T C_{in3} + L_P C_{d2}(L_N L_6 + R_1 R_2 L_6 C_{in3})) +$$
$$s^3(L_P C_{d2}(L_6 R_2 + R_T L_N) + L_M(R_2 L_6 R_1 C_{in3} + L_P L_N + R_2 L_P C_{in3} R_T + L_6 R_1 C_{in3}(L_P + L_N) + L_P L_N R_T C_{in3}) +$$
$$s^2(L_P C_{d2} R_T R_2 + L_M(R_T(L_P + L_N) + R_2 L_P) + R_1 R_2 L_6 C_{in3} + L_P L_N)L + s(L_M R_T R_2 + R_T(L_P + L_N) + R_2 L_P) + R_T R_2 \quad (18)$$

So the high-band resonant frequency can be approximated as:

$$f_H = \frac{1}{2\pi}\sqrt{\frac{R_T(L_N + L_P) + R_2 L_P}{L_6 R_1 C_{in3}(L_P + L_N) + L_P L_N R_T C_{in3}}} \quad (19)$$

It can be concluded that decreasing L_6 can move the low-band resonance frequency to higher frequencies as is confirmed in Fig.7. Also the values that are chosen for the elements makes the high band resonant frequency take place at about 9 GHz. Increasing R_2 and decreasing R_1 can also move the resonance frequency of high-band to higher frequencies, so that the gain can cover the whole wide frequency band.

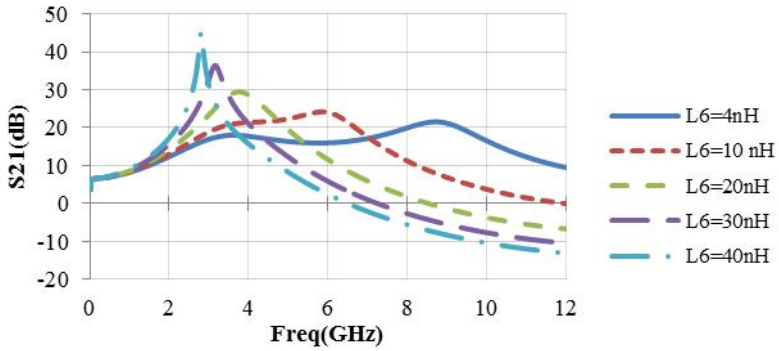

Fig.7. The efect of changing L_6 on high-band resonant frequency

4 SIMULATION RESULTS

In Radio Frequency systems especially in LNA design there are some parameters like gain, noise figure, stability, matching, and linearity that should be perfectly adjusted to achieve an appropriate performance. Actually there should be some compromises between these parameters because changing one of them can affect the others. So that achieving a relatively suitable result from each of them and consequently a whole suitable Radio frequency performance is of great importance.

At this part, first the table of elements' values is presented to provide a good perspective for the realization and implementation of the design and then the design parameters mentioned above are simulated and observed.

Table 1. The value of the elements.

L_1	**3.2 nH**	**R_1**	**20 KΩ**
L_2	0.15 nH	**R_2**	700 Ω
L_3	4.5 nH	**R_s**	25 Ω
L_4	18 nH	**W_{M1}**	28.9 µm
L_5	40 nH	**W_{M2}**	18.1 µm
L_6	3.9 nH	**W_{M3}**	21.7 µm
K	0.6	**W_{M4}**	28.7 µm
C_1	61 pF	**C_2**	68 pF

Gain, noise, input and output matching along with stability and linearity are simulated and observed in this section. The simulated S21 gain in depicted in Fig.8. It is obvious that the structure provides a relatively high and flat gain over the band of interest.

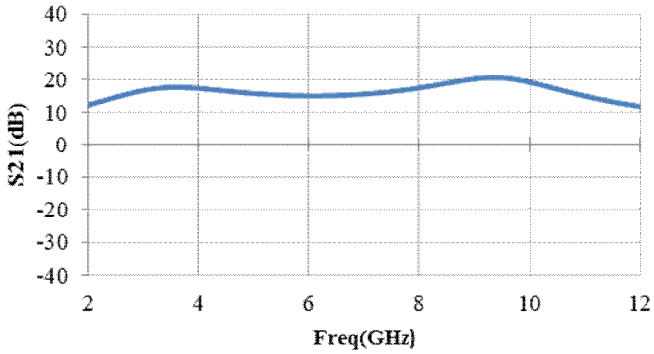

Fig.8. The S21 gain of the design.

The simulated minimum noise figure is shown in Fig.9, which illustrates that the structure has a minimum Noise figure lower than 1.7 dB.

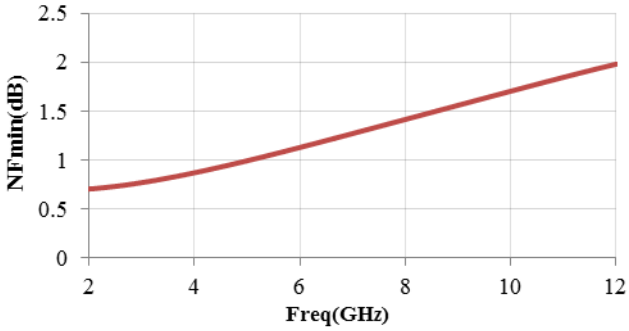

Fig.9. Minimum noise fiqure of the proposed LNA.

For the purpose of stability observation, stability factor (K) is illustrated in Fig.10. The stability factor is calculated using S-parameter simulations and its value which is larger than 1 across the whole bandwidth confirms the stable operation of the structure.

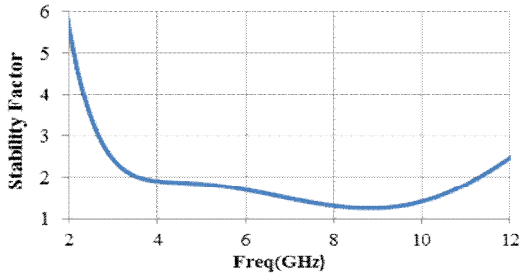

Fig.10. Stability factor of the proposed LNA.

Input and output matching are illustrated in Fig.11, in terms of S11 and S22 which verifies the matching of the design.

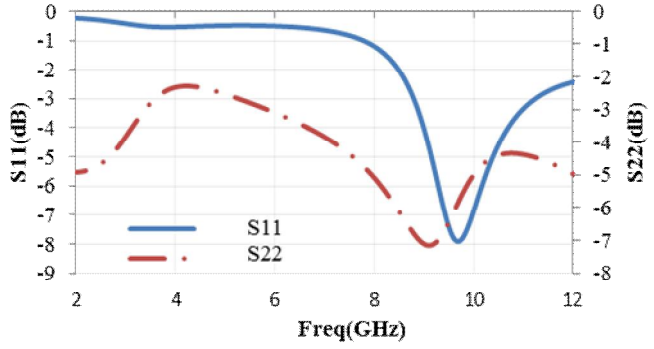

Fig.11. S11 and S22 of proposed LNA.

In order to take care of linearity of the design the third order intercept point is calculated at 6 GHz in Fig. 12, and the linearity is shown to be well provided.

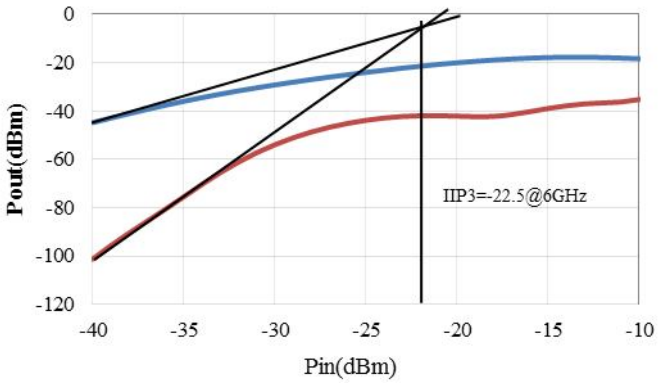

Fig.12. Third order intercept point.

Table 2 demonstrates the similarities and differences between some previously proposed structures. The design proposed in this paper covers the whole ultrabandwidth and it has the highest gain and lowest minimum NF. The linearity provided is much better than the others and power consumption is also the lowest comparatively. So that the comparison shows, that the proposed structure has been succesful to achieve a better performance than its counterparts.

Table 2. Comparison of Low power Low Noise Amplifier

	BW(GHz)	Gain S21 (dB)	MinNF (dB)	P_{DC} (mw)	VDD (v)	IIIP3 (dB)	CMOS Technology	Year
[2]	3–8	16.4	2.9	3.9	1.8	-	0.18 µm	2010
[4]	3.1 - 10.6	7-12	5.27	4.5	1.5	-2. 23	0.18µm	2010
[5]	2.6-9.2	10.9	3.5	7.1	1.8	-5.1	0.18 µm	2005
[6]	3.1-10.6	17.5±1	2.25	10.6	1.8	-	0.18 µm	2009
[8]	1-10	10.5	4.2	12.65	1.5	-	0.18 µm	2009
[12]	3.1-10.6	13.5-16	3.1	11.9	1.8	-7	0.18 µm	2007
[13]	3–5	15	3.5	5	-	-	0.18 µm	2010
[15]	3.1-10.6	14	4.5	21	1.8	-12	0.18 µm	2010
[16]	0.1-10.6	12	3.8	9.8	1.8	-	0.18 µm	2007
This work	3.1-10.6	16-20	<1.7	3.4	1.8	-22.5	0.18 µm	

5 conclusions

An ultrawideband low noise amplifier is proposed in this paper. The design is consisted of two stages, a cascode structure along with a buffer stage. The gain and resonance frequencies are formulated and the design parameters are simulated. The design is based on 0.18µm CMOS technology. The simulation results approve the desirable application of this structure in UWB. A high flat, and wideband gain about 20 dB is achieved. Low noise characteristic is confirmd by a minimum noise figure lower than 1.7 dB. The significance of the proposed LNA gets more obvious considering that these all desirable characteristics are provided in the case that the whole power consumption of the design is 3.4 mw. This is very important specially for integration concept where low cost and low power dissipation is very magnificant.

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