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A Novel Structure for CCII Based SC Integrator Based on CCII with Reduced Number of Switches

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ABSTRACT

This paper describes a new switched-capacitor (SC) integrator. This integrator not only has the advantages of conventional opamp based integrators but also has the capability of switching in high frequency due to inherent characteristics of second generation current conveyor (CCII). To implement integrator, 7 switches and non-overlapping clock are used. Time shared use of internal CCII buffers is performed to make input output transfer function. The circuit is simulated by means of HSPICE and WAVEVIEW to confirm theoretical results in 0.35µm technology.
Key Words: Integrator, SC Circuit, Current Conveyor, 'Low Pass Sigma Delta Modulator' (LPSDM), CCII.

1. INTRODUCTION

Sigma-Delta Switched-capacitor circuits have been widely used for implementing monolithic filters. The long time interest in the design of SC filters is motivated by the fact that such filters can be realized using standard CMOS digital process technologies. This is due to availability of high performance opamps as well as high quality MOS capacitors and switches.

An SC building block that is useful in implementing SC filters is the SC integrator [1]. It can be shown that (in the ideal form) the transfer function of an SC filter depends on switching frequency and the ratios of capacitance values [2]. These capacitive ratios can be obtained and maintained to accuracy much better than 1% over a wide range of temperatures and of signal amplitudes [3].

For these reasons considerable effort has been directed toward developing high performance circuits and devices for SC filters.

Traditionally opamps have been used in SC integrator realization for more than three decades [4]-[7]. Also some little efforts have been done to design and implement SC integrators using voltage buffer [8]-[11]. Therefore it is possible to replace opamps by other unity-gain devices. More recently a current mode building block named CCII has been introduced [12]-[13]. It has the advantages of higher speed, slew rate and wider dynamic range of current mode circuits [12]. Although CCII had been introduced in 1971 but synthesis and design methods are not mature, especially for the SC circuits realizations. It seems there is very little concern about CCII based SC circuits in the literature. Due to the inherent high frequency capability of CCII building block [12] it is an attractive candidate for replacing opamps in the integrator circuits. Furthermore, CCII does not need external feedback and hence no stability problem [13].

For the first time Maundy and his colleagues have shown that it is possible to realize SC circuits using CCIIs without requiring circuit transformation [14]-[15]. They employed miller theorem to replace feedback capacitor C2 in an SC opamp based integrator by a grounded capacitor of equal value connected to the Z terminal of CCII. Fig. 1 shows this process.

In a recent effort, some other CCII based SC integrators have been proposed [16]. As it is shown in Fig. 2, these works were based on realization of RC prototypes with required characteristics and transformation of the resulted circuits to their SC equivalents [17].

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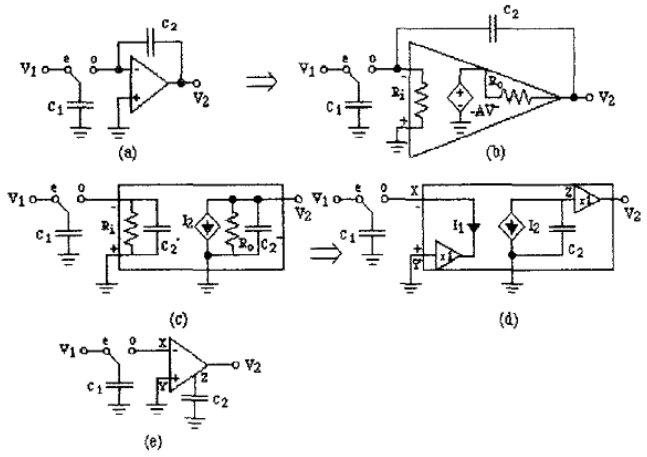

Fig. 1 *The derivation of SC CCII integrator by Millers theorem.*

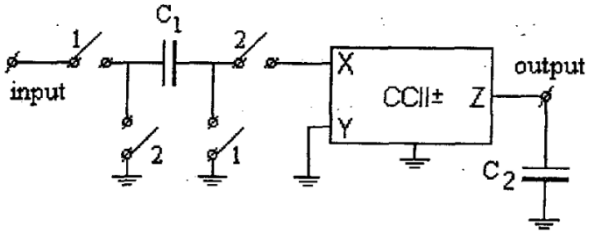

Fig. 2 *An integrator with Realization of RC prototype with their SC equivalent.*

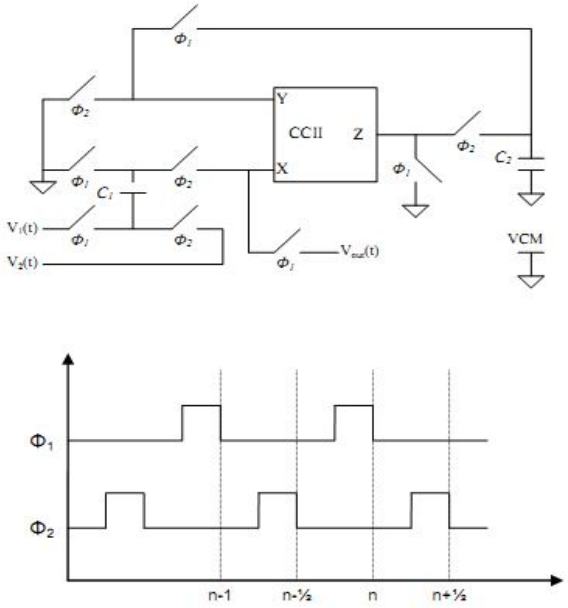

Fig. 3 *The CCII based SC integrator by eliminating extra voltage buffer.*

A common drawback in these works was the need for the voltage buffer at the output of the circuits to cancel the loading effects of the next stages. This led to use of an extra voltage buffer in addition to the CCII (see Fig. 1d). Thus it seems that not a pure CCII based circuit is realized.

In a more recent work a novel structure has been proposed which eliminates the need for extra voltage buffer [18]. This integrator followed by clock pulse scheme is shown in Fig. 3. It is based on time shared use of internal buffers of CCII.

All these efforts to realize integrator by CCII are based on various topologies including: 1) input signal is connected to Y and output is connected to Z [16], 2) input signal is connected to X and output is connected to Z [16] and finally 3) input and output are connected to X [18]-[19].

This paper proposes a novel architecture using Y terminal as input and X terminal as output [20]. The proposed integrator has the all advantages of previous CCII based integrators. It seems to be less noisy in compare to [18], because of reduced number of switches [1].

2. PROPOSED INTEGRATOR

The circuit followed by its clock pulse is shown in Fig. 4 [20]. To realize integrator, time sharing of internal CCII current and voltage buffers are used. In the following formulas, 'o' and 'e' indices are the symbols for odd phases (φ1) and even phases (φ2), respectively [1]. Assume that the time of charge and discharge of capacitors are insignificant compared to clock pulse periods.

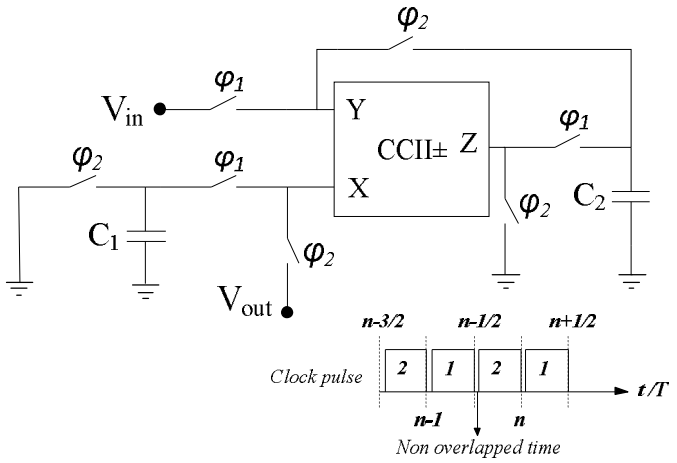

Fig. 4 *The proposed integrator followed by clock pulse scheme[20].*

Hence one can results that the charge on C2 in n-3/2 (immediately after shutting off the φ2, ignoring non overlapped time) is equals to the charge which is stored on output (X terminal) at n-1 (immediately before shutting off the φ1 or opening the φ2, ignoring non overlapped time). Besides, there is no change in output after shut off the φ1, so it can be shown that:

$$(n-\frac{3}{2})T < t < (n-1)T : C_2 V_{out}^{o}(n-1) = \pm Q_{C2}^{e}(n-\frac{3}{2}) \tag{1}$$

During odd phases (see Fig. 5a), input signal is connected to Y terminal so that its voltage will be transferred to X terminal through internal voltage buffer of CCII. Therefore the charge stored on C1 becomes:

$$(n-1)T < t < (n-\frac{1}{2})T : \quad Q_{C1}^{o}(n-1) = C_1 V_{in}^{o}(n-1) \tag{2}$$

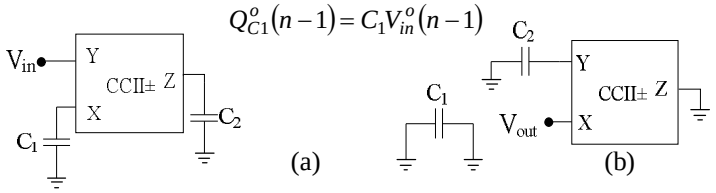

Fig. 5 *The proposed integrator at a) phase φ1 and b) phase φ2*

At the same time, sampling and integrating capacitors are connected to X and Z terminals, respectively. The charge stored on C1 is transferred to C2 via internal current buffer of CCII. At the next phase (see Fig. 5b) integration capacitor is connected to Y terminal and transfers the charge stored of previous phase via internal voltage buffer of CCII:

$$(n-\frac{1}{2})T < t < nT : C_2 V_{out}^{e}(n-\frac{1}{2}) = Q_{C2}^{e}(n-\frac{1}{2}) \tag{3}$$

It is worth to mention that in this phase, the Z terminal is tied to ground to prevent the Cz parasitic capacitance being charged. It is assumed that the Y terminal has no significant effect on C2 hence doesn't perturb its charge while connected to Y terminal. Thus the charge stored on C2 transfers to output. Based on this concept, C2 holds the charge of two preceding pulses:

$$Q_{C2}^{e}(n-\frac{1}{2}) = Q_{C1}^{o}(n-1) + Q_{C2}^{e}(n-\frac{3}{2}) \tag{4}$$

Substituting (1) and (2) into (4) and put the result into (3), results in:

$$C_2 V_{out}^{e}(n-\frac{1}{2}) = \pm C_1 V_{in}^{o}(n-1) + C_2 V_{out}^{o}(n-1) \tag{5}$$

As was mentioned before, it is assumed that the charge during each phase remains unchanged thus there is no change in output after shut off the φ_1, so it can be written that:

$$nT < t < (n+\frac{1}{2})T : V_{out}^{o}(n) = V_{out}^{e}(n-\frac{1}{2}) \tag{6}$$

Substituting (6) in (5), the integrator's input-output relationship will be obtained in time domain. It is shown in (7).

$$C_2 V_{out}^{o}(n) = \pm C_1 V_{in}^{o}(n-1) + C_2 V_{out}^{o}(n-1) \tag{7}$$

Arranging (7) and then using of Z transform, the transfer function of integrator will be proved, which is shown in (8).

$$H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \pm \frac{C_1}{C_2} \frac{Z^{-1}}{1-Z^{-1}} \tag{8}$$

The ±sign is due to use CCII- and CCII+, respectively.

3. **SIMULATION RESULTS**

The simulation was done for the proposed integrator based on a CCII- [21] which is shown in Fig. 6. This CCII- is simulated in 0.35µm technology [22].

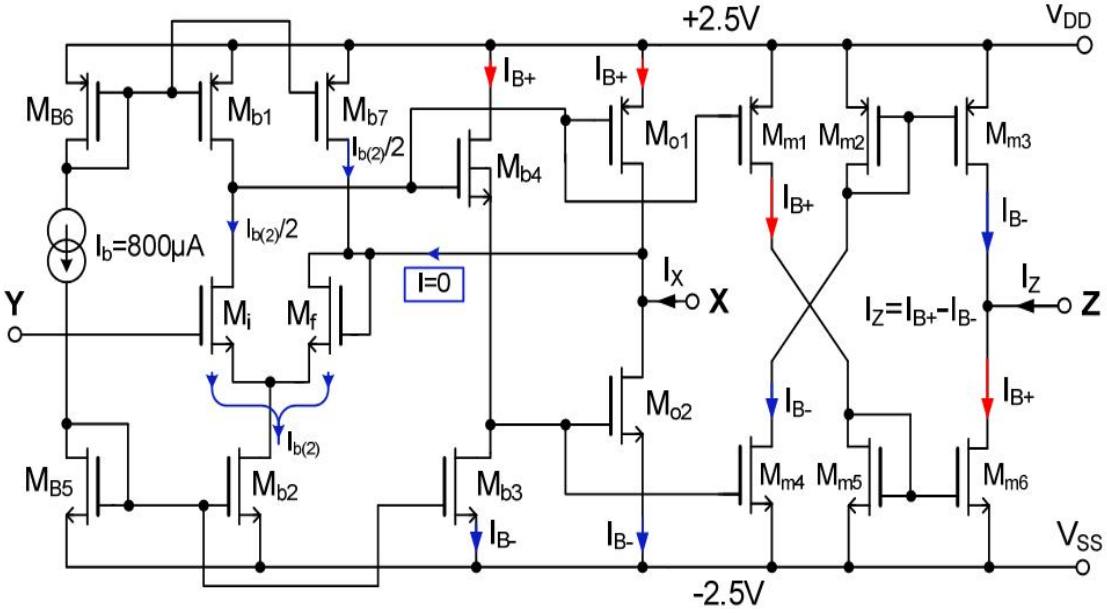

Fig. 6 *The circuit of CCII-.*

The curves of voltage and current buffers of CCII- are shown in Fig. 7 and 8, respectively. One can results that the errors from the ideal gains for voltage and current are less that 0.5% and 1.8%, respectively, over a frequency range from 0 to 10MHz. Therefore the gains are so close to 1.

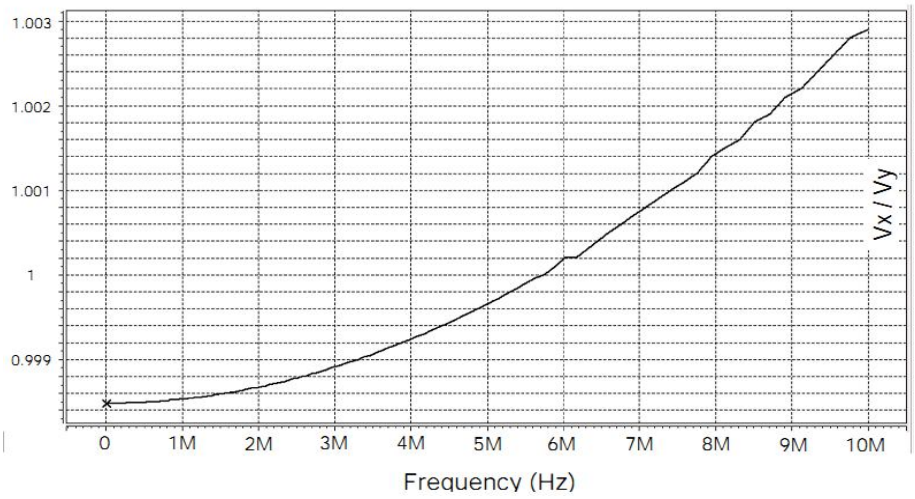

Fig. 7 *The voltage gain of the voltage buffer of CCII-.*

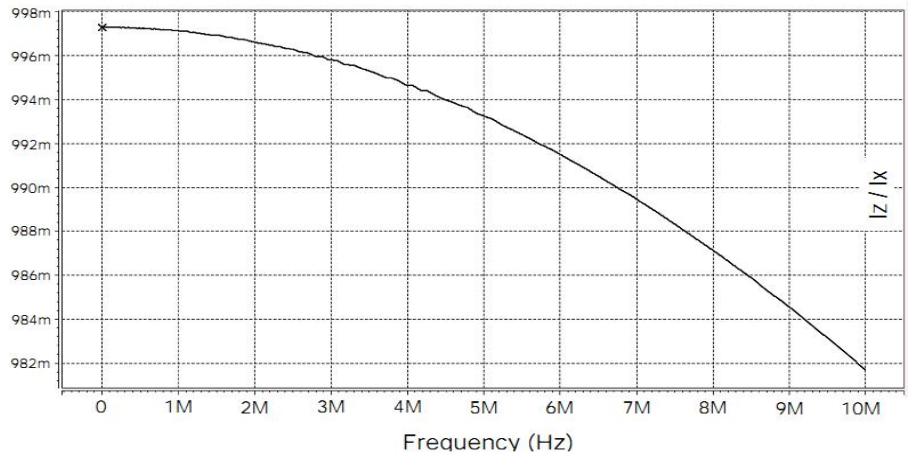

Fig. 8 *The current gain of the current buffer of CCII-.*

Voltage controlled resistors were used to model switches. The amplitude and the frequency of input signal were 0.9 V and 1 MHz, respectively. The sampling frequency was 10 MHz. The was done by means of HSPICE. The input-output signals of the integrator are shown in Fig. 9. The dotted line is input and the solid line is output. The output has 90 degree delay with the input signal which denotes the integrating process of the integrator.

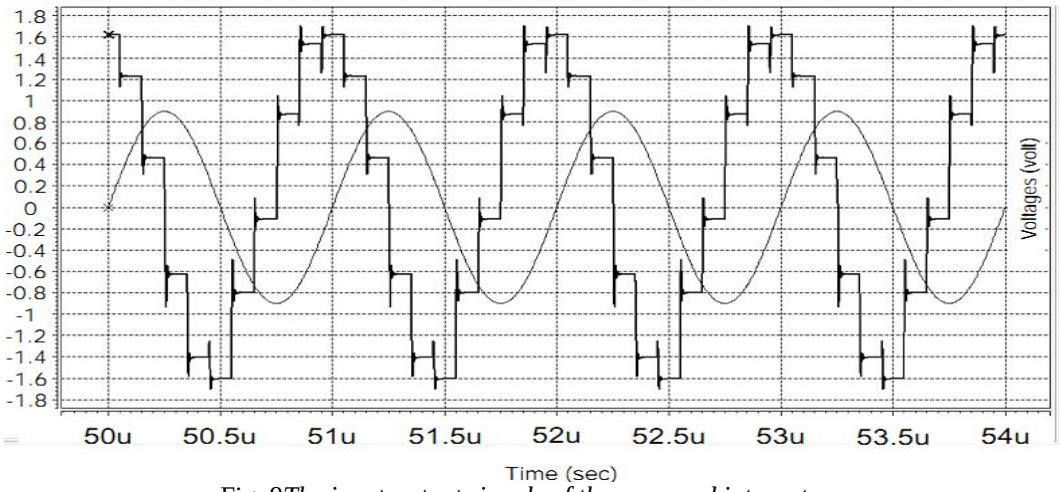

Fig. 9*The input-output signals of the proposed integrator.*

3. CONCOLUSION

A novel CCII based SC integrator is proposed. The analysis of the circuit is carried out. It seems to have similar equations as traditional opamp based integrators. The number of switches is minimized.

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