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Generating New Reversible Logic Gates with Ladder Block Structure for Emerging Nanocircuits

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ABSTRACT

Reversible computing is an emerging scene of research and reversible logic synthesis is its significant aspect. The present study aims to generate the reversible logic gates with new outputs that never been seen. In this paper, the schematic diagram with minimum quantum cost for reversible gate and combination of several quantum gates is considered. I illustrate that we can displace control-bit and target-bit in Feynman gate and produce EXNOR gate in output. Also, N number of ladder Feynman gate can produce (N+1)EXOR gate without any garbage output. The new reversible logic gates from FG, F2G, PG, TG, BVF, R and TR gates is generated. Sometimes, the available gates are from the same kind and can extract an ideal output, though we should consider the speed and the wasting power. The resulting ladder gates realization has been depicted in the following figures. All the results verify with the truth table. This work with recently outputs introduced for the first time.
KEYWORDS: Reversible Logic Gates, Quantum cost, Ladder quantum gates.

INTRODUCTION

In recent studies, Reversible Logic is becoming one of the potential power optimization techniques in Low Power CMOS circuits, and also finds its application in optical computing and Nanotechnology. Quantum gates are significant part of quantum communication and computation. Each reversible circuit has a one-to-one correspondence between inputs and outputs and there is the same number of inputs and outputs .Theoretically, these computation are called reversible because there is no data loss. The output lines being not required in the original function may become visible. These lines are called garbage lines.

As the complexity of applications grows, power dissipation of VLSI chips becomes one of the crucial aspects. In mobile devices, for example, high power dissipation decreases the battery lifetime. Reversible computing is motivated by the Landauer principle, which proves that irreversible logic operations must incur a fundamental minimum energy cost[1].Bennett demonstrated that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. For irreversible logic, each bit of information lost produces kTln2 Joules of heat energy, where k is Boltzmann's constant and T is absolute temperature at which the computationis performed. For room temperature T, the amount of heat dissipated for one bit is small i.e. 2.9×10^{-21} J [3].Given a reversible function, the quantum logic synthesis problem is to synthesize the function using the elementary quantum logic gates with the minimum cost. Various heuristic methods have been applied to find low cost quantum implementations (using the elementary gates) for the functionality of the Fredkin, Toffoli and Peres gates[4].The reversible gates utilized to design the conventional logic are so chosen to minimize the number of reversible gates used and garbage outputs generated. The classical logic gates such as AND, OR, NAND, NOR, EXOR and EXNOR are not reversible, but we can generate these outputs using reversible logic gates[5].

BASIC REVERSIBLE LOGIC GATES

There are a number of existing reversible gates in literature. The most well-known (2, 2) reversible gate is the Feynman gate. If *n*-input *n*-output logic function $f : \{0, 1\}^n \rightarrow \{0, 1\}^n$is bijection, it is reversible. For example 2-input 2 output function (x1, x2) → (x1, x2 ⊕ x1) is reversible. Feynman gate(CNOT gate) and Toffoli gate are shown in Fig.1.

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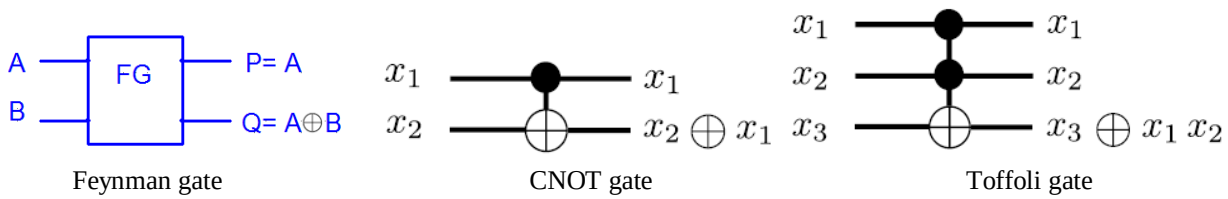
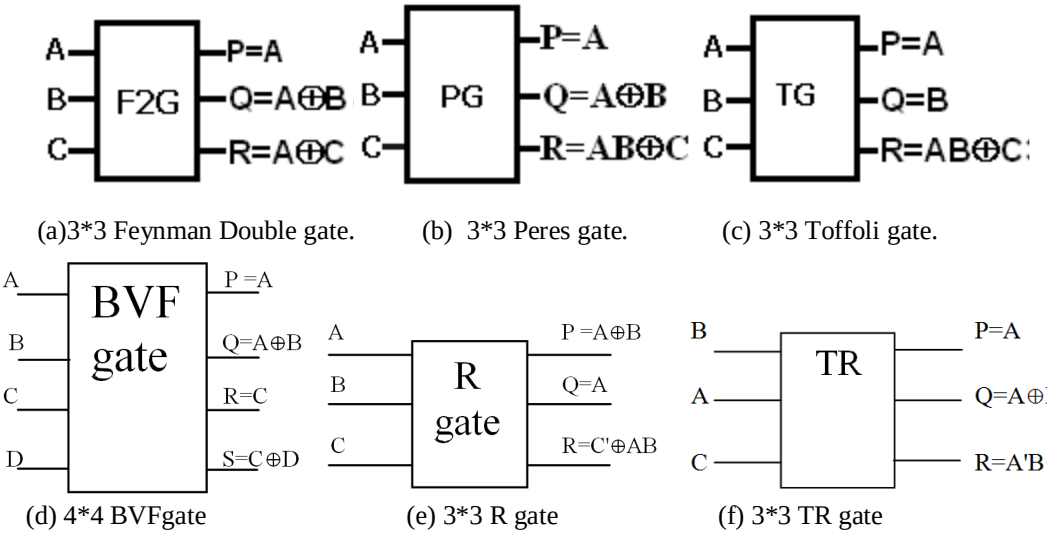


Feynman gate CNOT gate Toffoli gate

Fig. 1. The reversible logic gates[6]

In Feynman gate, one of the input bits act as control signal (A). That is, if A= 0 then the output Q follows the input B. If A = 1 then the input B is flipped at the output Q. Because of this, it is called as controlled NOT (1-NOT) and also called asquantum XOR because of its popularity in the field of quantum computing[7].Fig. 2 shows the F2G gate[8] and the Peres gate[8] and the Toffoli gate[8] that Each of these gates is universal .Also, BVF gate[9] and R gate[9] and TR gate[10] are shown in fig2. Generally, some well-known reversible logic gates are shown in fig2.

Because of their easinees and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other. The quantum cost of a reversible circuit is the number of primary quantum gates required to implement a circuit.These gates is one-through gate which means that one input variable is also output. Although, These gates is very noticeable since it does not introduce garbage outputs or less garbage outputs.



(a)3*3 Feynman Double gate. (b) 3*3 Peres gate. (c) 3*3 Toffoli gate.

(d) 4*4 BVFgate (e) 3*3 R gate (f) 3*3 TR gate

Fig. 2. Some well-known reversible logic gates [8],[9],[10].

REVERSIBLE LOGIC SYNTHESIS

Reversible logic synthesis is not as easy as classical logic synthesis. The major constraints of reversible logic synthesis are: (i) the fan-out of every signal, including primary inputs, is one, (ii) the graph of the reversible circuit must be a dag (directed acyclic graph), which means that there must be no loops of gates or internal loops in a gate, and (iii) many of the practical functions are not themselves reversible and need to make reversible before implementing them with reversible gates[11]. Such a variety of different reversible gates results in a variety of different approaches to reversible logic synthesis. by analyzing theconditions that affect the number of garbage outputs. Minimization of garbage outputsmay be even more important for some technologies than minimization of the number of gates[3]. Similarly, By minimizing the quantum cost we can achieved the optimization quantum gates.

Real quantum cost for a realtechnology is different, but research laboratories who possess tools for real quantum cost calculation do not want to share the information (partially because their quantum cost calculation are

designed specifically for their unique equipment) [3]. The detailed cost of a reversible gate relies on any particular realization of quantumgate.

NEW REVERSIBLE LOGIC GATESWITH MINIMUM QUANTUM COST

Because of reversibility characteristics, it is easier for reversible circuits than for classical circuits. In this section, I introduced several new reversible logic gates with minimum quantum cost. Firstly we have suggested FG with 3 more QC. The outputs of this gate isshown in fig 3. One of the characteristics of this circuits is that the place of the control bit and the target bit is switched. Also, Double Feynman gate with 2 more QC is shown in fig4.

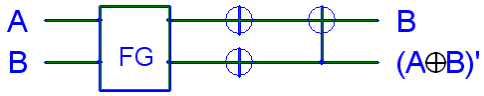


Fig3.FG with new outputs

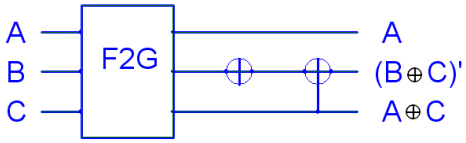


Fig4. F2G with new outputs

We can achieve the following outputs by using the PG, TG, BVF, R and TR gates respectively. The results are shown for following gates similarly.

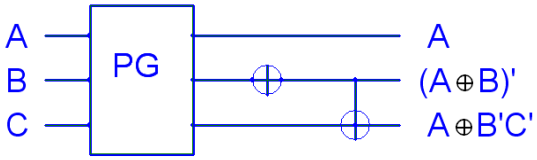


Fig5. PG with new outputs

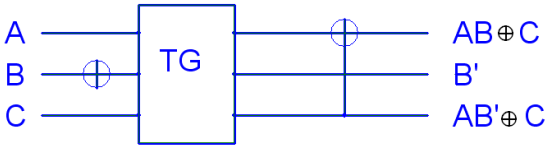


Fig6. TG with 2 more QC

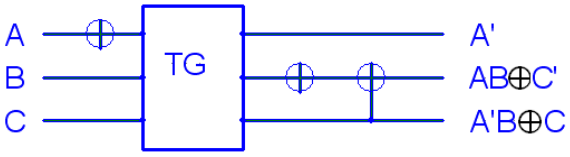


Fig7. TG with 3 more QC

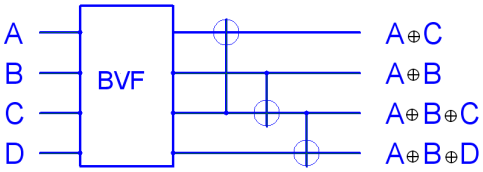


Fig8. BVF gate with new outputs

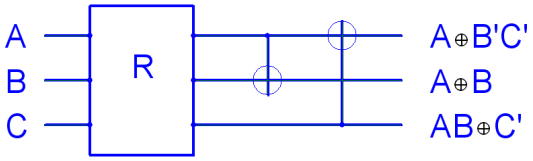


Fig9.R gate with new outputs

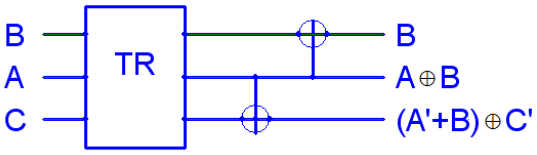


Fig10. TR gate with new outputs

As can be seen, using this method can be implemented in the future quantum circuits with minimum quantum cost. Furthermore, it is necessary to compare the results of recently studies of the quantum circuits to produce the best possible circuit with the desired outputs. We were able to synthesize more complex circuits that had not been shown previously.

LADDER BLOCK STRUCTURE OF REVERSIBLE LOGIC GATES

In this section, we introduce ladder block structure of reversible logic gates that is shown in following figures. For example, ladder Feynman gates with those outputs is shown in fig 11.Final outputs are A⊕B⊕C and

A⊕B⊕C⊕D respectively number of ladder Feynman gate can generate (N+1)EXOR gate without any garbage output.
Depending on the necessary outputs we can use the following blocks. We have often used D,E inputs and often used 0,1 inputs.

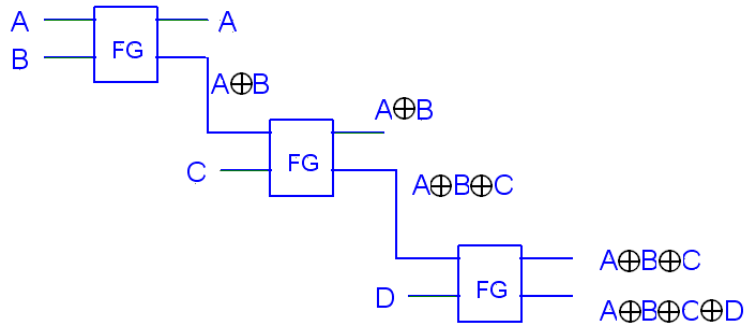


Fig11. Ladder block structure of Feynman gate

Also, An efficient analysis for F2G was presented that new ouputs is shown in fig12.

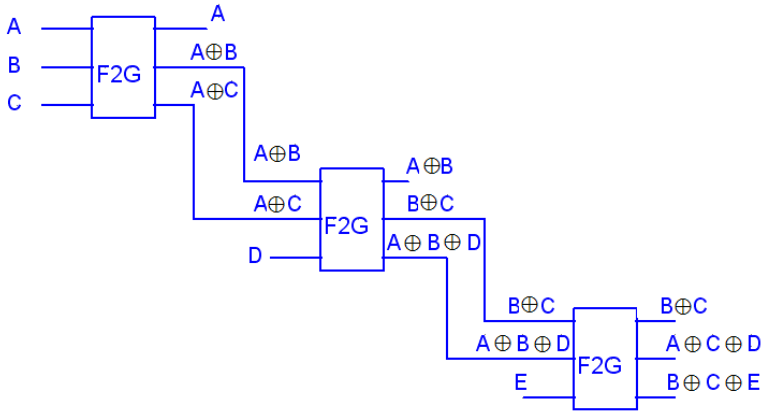


Fig12.Ladder block structure of F2G gate

The results for the PG,TG, BVF, R and TR gates are shown in fig 13,14,15,16 and17respectively.

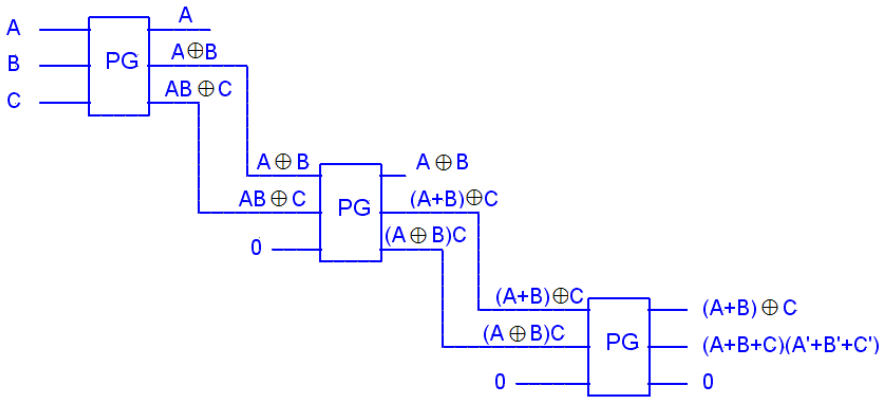


Fig13.Ladder block structure of PG gate

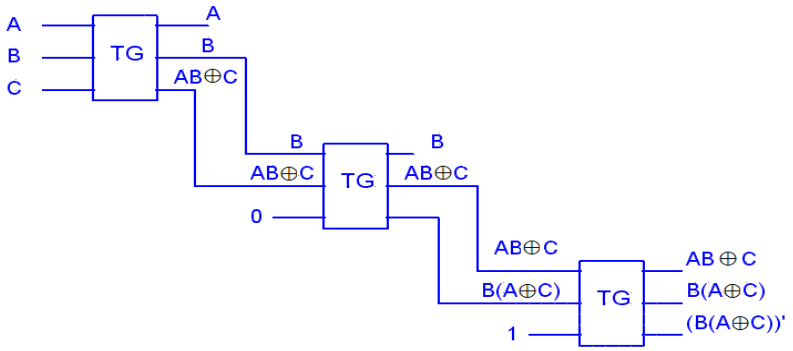


Fig14.Ladder block structure of TG gate

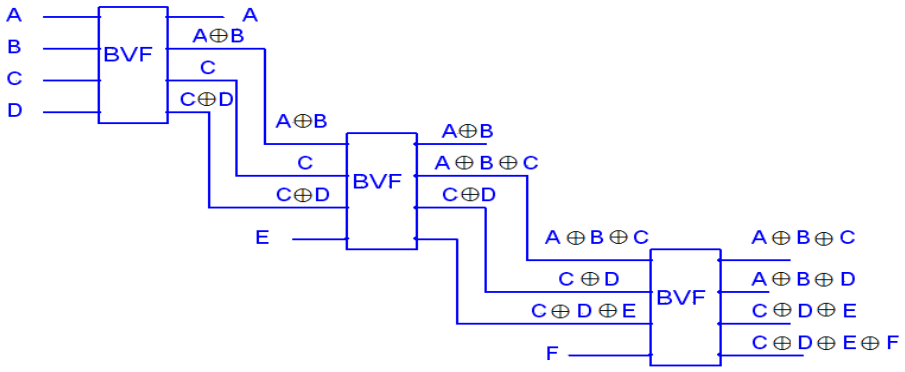


Fig15.Ladder block structure of BVF gate

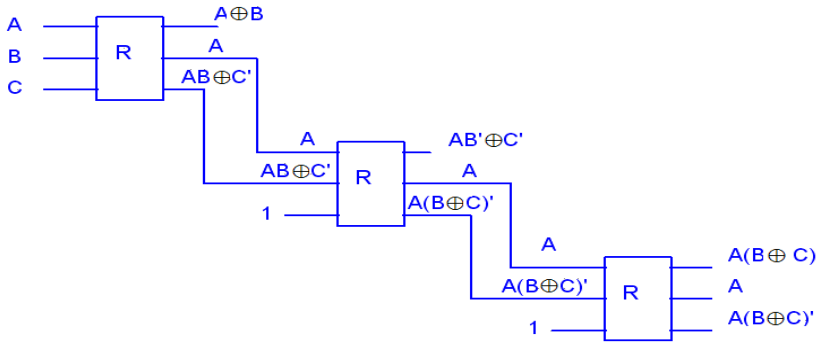


Fig16.Ladder block structure of R gate

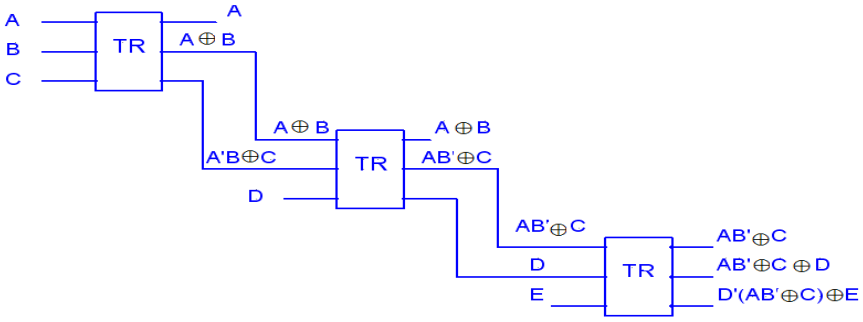


Fig17.Ladder block structure of TR gate

We have shown that the ladder block structure of mentioned gates can be used for all over the same reversible logic gates. However, various non-identical gates can be considered as well as. The goal of our approach is not only to several quantum gates, but mainly to demonstrate various configuration and structure of reversible and quantum circuits synthesis extensively.

CONCLUSION

The main goal of this paper is finding a good architecture for ladder quantum gates based on minimizing garbage outputs and availability of same gates. In each block calculates the logical outputs that is the logical inputs for the next block. Depending on the type of outputs that need we can be able to produce these gates. We generate desirable output values from the each block size, which is exemplary various outputs. Also, we present a new reversible logic gates from the basic reversible gates that it consists of minimum quantum cost with ultimately 3 more QC. Therefore, many of the new reversible gates can be generated with a little change to introducing efficient outputs among the functions that rarely seen. All the results have been verified by the truth table. An application of the proposed gates are in emerging technologies and QCA nanotechnology.

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