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Analysis and Description of Binary Mathematical Model PLL Its Function and Behavior

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ABSTRACT

PLL performance as a basic block has a great impact on system performance. Thus, high-performance phase locked circuit design has always been desired by researchers and designers of electronic systems and telecommunications. Bang-bang phase locked loops used today in high-speed systems has increased dramatically. Since the PLL phase lock, so step input phase behavior of the system can be a criterion to predict the behavior of such structures is stable and fast. Binary Phase-Locked Loop as a non-linear system, a different response in the phase and frequency of exposure to the entrance stairs. In this study, the behavior of the system in response to a step input frequency is investigated. The lock and capture range of the PLL in this study is very important that this issue is addressed. Furthermore, this study since all the features are Extraction system transient including lock time. To analyze the behavior of the loop in response to a step input frequency, the PLL output is a mathematical model and the characteristic time-locked, get up suffering as well as slipping a relationship to predict the occurrence of adverse cycles are extracted.

KEYWORDS: binary phase-gate, XOR detector Alexander, binary mathematical model, block detector, MATLAB software

1. INTRODUCTION

Phase locked loops are used in large utility blocks on communication circuits, as transponders RF, wireless and fiber-optic receivers are [1- 4]. Among the most important application of phase-locked loop as a basic block frequency modulation, frequency synthesizer and clock data recovery circuits (CDR) is [5-11]. Although the basic structure remains the same lock ring, however, its implementation in different technologies is still for various applications such design problems. Here are two important factors in the development of phase-locked loops noted.

The first factor, the demand for high-performance and low-cost electronic systems, and the next, advances in technology and manufacturing of integrated circuits [1-3, 5]. One of the main reasons that the use of non-linear PLL including binary phase locked loop (bang-bang) has increased the use of this type of CDR PLL in high-speed circuits. A PLL phase detector for detecting a phase difference needed to identify the phase of the input and output.

We expect a phase detector that produces a control signal, the output frequency is changed so that the frequency is equal to the input frequency. It should be introduced first block, the block detector (PD). A phase detector can be linear or nonlinear structures. Linear phase detector output (V_{PD}) is equivalent to:

$$V_{PD} = v_{cot} = (\varphi_{in} - \varphi_{out})K_{PD} \quad (1)$$

Where K_{PD} is the phase detector gain, In fact, we can say that the phase detector output is linearly correlated with the phase ring, therefore expected to increase phase, the output pulse width increases. One of the simplest linear phase detector, is an XOR gate [2, 5]. Construct an XOR gate with input and output waveforms in Figure 1 is shown. From Fig. 1 it is clear that the mean value of the control voltage (dc) is obtained as follows: . $\Delta\varphi$

$$\overline{V_{PD}} = \overline{v_{cot}} = \frac{A.\Delta\varphi}{\pi} = K_{PD} \quad (2)$$

Including A / π represent the voltage level of the control period and a $K_{PD} = A/\pi$ phase detector is used. As can be seen, a linear relationship exists between the average values of the control phase.

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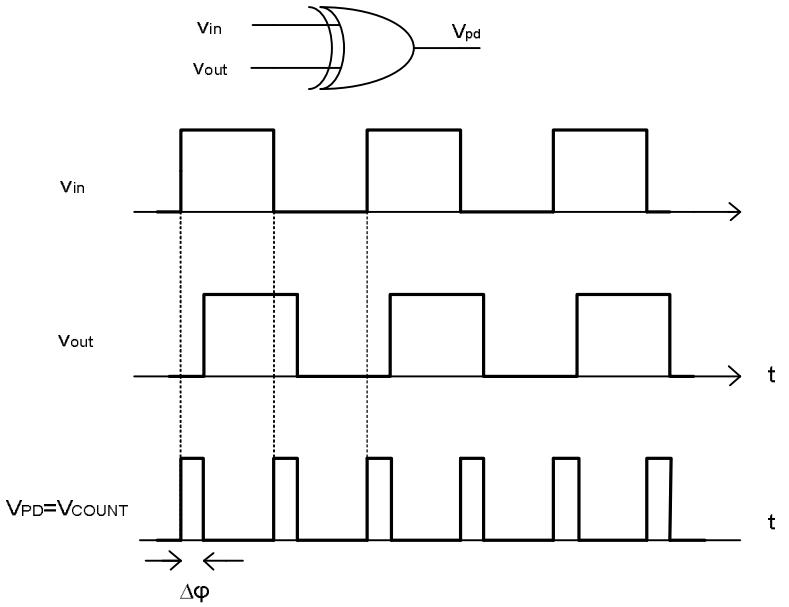


Figure 1. XOR gate and its function as a phase detector.

Today's high-speed digital applications telecommunications data is increasing dramatically [12-14]. The orientation of the optical telecommunication and doing a lot of research is the analysis and design of high-speed circuits. Because the clock and data recovery circuit analysis and design with the desired characteristics is one of the main challenges in high speed communication systems, the main objective of this research is the type of circuit. Phase loop using linear detectors relative to meet the needs of a system. But for uses of high speed PLL detector based on binary (bang-bang) is used. Because the PLL phase detector linearity, if any, due to linearity, pulse output proportional to the phase difference, but if the frequency is high, it the input data rate is high, the output pulse width is very narrow. This research work is based PLL bang-bang high-speed applications.

2. The Available Challenges

In general, the analysis of one-loop bang-bang phase can be divided into two major challenges, the first being BBPLL due to non-linear detector, we cannot analyze the concepts of linear control systems used in phases. In BBPLL ultimately "non-linear equations, whose solution will be very time consuming and difficult, there are challenges in BBPLL Analysis of Jitter. Due to nonlinear BBPLL Jitter Analysis of PLL Jitter analysis of the much more difficult is linear. Goal of Jitter is to analyze the bit error rate (BER) does not exceed its limit. Therefore we can say that the non-linearity factor BBPLL rise to two main challenges.

3. Simulating Proposed Relations

MATLAB software is used for simulation. Using software simulation environment, we BBPLL structure. In this paper, we first introduce the blocks used in simulation, After introducing the simulation model to evaluate the accuracy of the phase detector instead and we will investigate the behavior of the system to step input phase. The results are compared with simulation results. Furthermore, the results obtained in response to a step input frequency were studied and the simulation results are compared.

3.1. Simulated Block Structure BBPLL in MATLAB

This section introduces the blocks used in the simulation process. In BBPLL Alexander phase detector simulation is used. Nand gate-level simulation of the detector has been used. Thus, the entire block detector used in the XOR and the D-Flip-Flop from Nand gates are used.

3.1.1. XOR Gate

Here Nand gate because the use of a gate, XOR gate, if all Nand we implement as well. This is shown in Fig. 2.

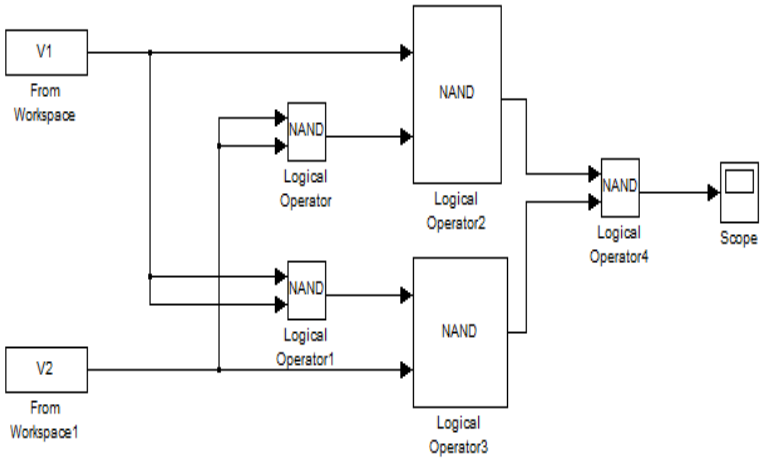


Figure 2. XOR gate using basic gates Nand

XOR gate with two inputs v_{in1} and v_{in2} and performance, we have simulated in Fig. 3, the results will come. As we know, the output of this gate for two inputs (0 or 1) is always zero for two inputs and one will always be unequal.

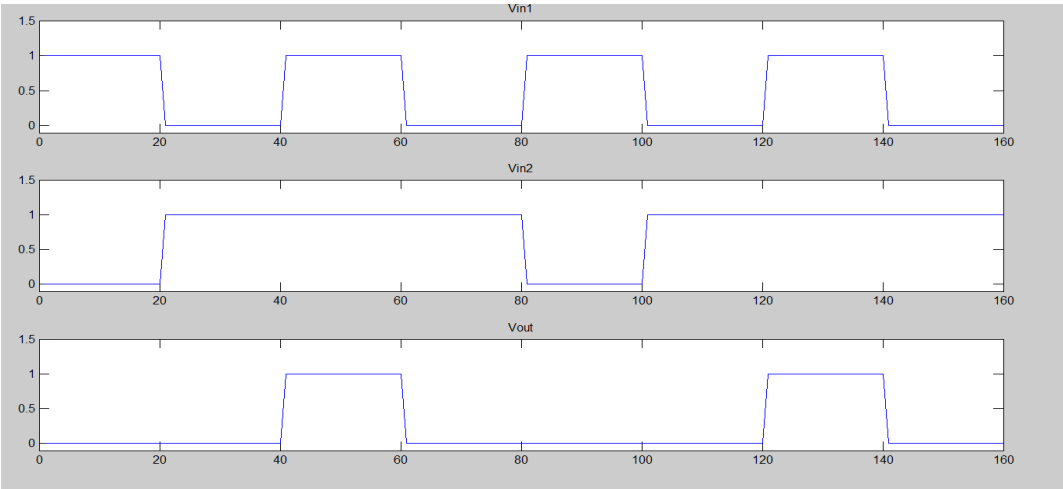


Figure 3. Simulation results of the XOR gate

3.1.2. Performance Simulation of D-Flip-Flop

All of a D-Flip-Flop clock rising edge sensitive Nand use. It is also clear that the primary outlet for converging basic dc output Preset, Clear is used. Therefore, the three-input Nand gates need. To investigate the function of the clock frequency GHz 1 is used. Time is up for proper $\overline{Ctr} = '0', 0.5nt$ operation. To the initial moment, the output value is specified. Well as for the normal functioning of the D-Flip-Flop, $\overline{\Pr e} = '1'$ we choose. D-Flip-Flop sensitive to rising edge, the rising edge of the input clock sensitive and immediately view the input (Q) and moves to the next rising edge continues.

3.1.3. Alexander Detector Simulation

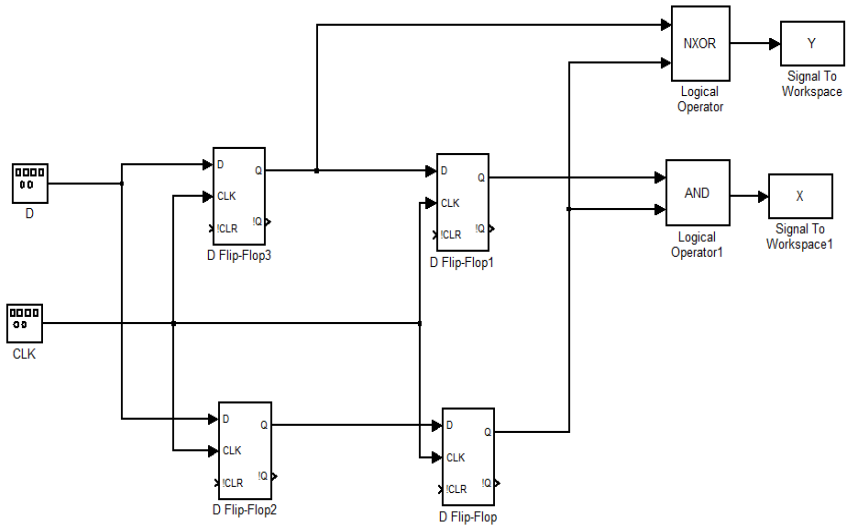


Figure 4. Structure detector Alexander

In this phase the simulations we have done in the previous step, the binary detector simulation discussed Alexander. Fig. 4 Complete the diagram of the detector have shown Alexander. . Fig. 5 shows that late in the detector output. The simulation is similar to D-Flip-Flop is always up for a good performance $\overline{Ctr} = '0', 0.5ns$ and $\overline{\Pr e} = '1'$. As can be seen in this figure, the clock (CLK) input data (D_{in}) falls behind; outputs activated late and early output remains zero.

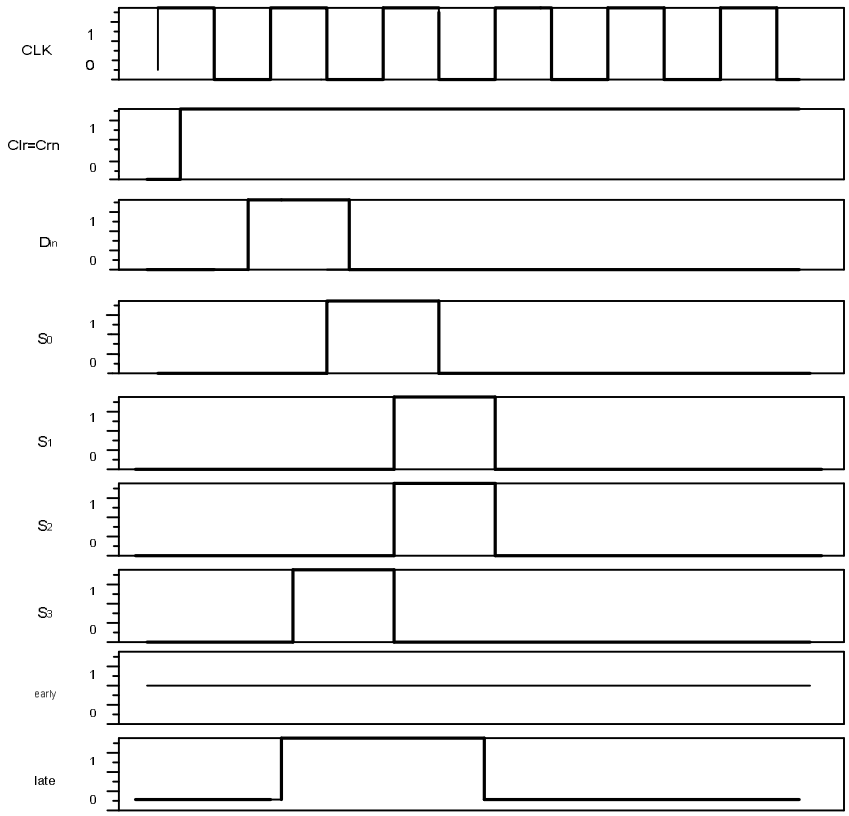


Figure 5: The output waveform of late

3-1-4. Simulating Load Pump

Charge pump current source used in the simulation must be input voltage can be controlled. Thus, the voltage-controlled current source have used the phase detector is the input pulse. In this case, the first order filter consisting of a resistor and a capacitor to discharge and charge pump phase detector block is added to the input. The simulation block voltage measurement, measurement current is used to measure voltage and current. To determine the value of the current block, important direct current source, connect the output of the phase detector is a current source. Use the sources and leads in this case it is difficult not to conclude an acceptable answer. Thus, the output of late, early, and the little time we add input current source, it is exactly like that of the input voltage controlled current source can be used. The detail of the governing equations shows a linear oscillator. The relationship between oscillator frequencies $\infty_{cu} = \infty_{u} + R_{nc}V_{ct}$ is exactly the same. Conditions are simulated with the above mentioned methods proposed in this research.

4. Simulating Results of the Analysis of Transient Behavior BBPLL to Entrance Stairs Phase

The entrance stairs to phase BBPLL analysis must consider two cases. BBPLL the case without oscillation output phase lock mode is the so-called stability factor BBPLL great. The latter occurs when the swing to the point of having a lock is BBPLL know that large off-chip capacitor is mounted on a circuit that does a high volume occupied. Fluctuations in the transient state equations are derived for the case that the major factor is the stability of the system is no fluctuation could also explain its behavior.

4.1. Simulation of Transient Behavior BBPLL Stairs to Phase Input or a Large Stability Factor

To start the simulation, the following parameters are used.

$$R_p = 300\Omega \qquad l_p = 40\mu A \qquad K_{ocp} = 200MHz/v \qquad C_p = 5nf \qquad \Delta\varphi_{in} = irad$$

In this case, the stability factor is as follows:

$$\zeta = \frac{2R_pC_p}{t} = 6000 \tag{3}$$

Add additional output phase and phase difference, respectively, were obtained as follows:

$$\varphi_{out,ex} = \begin{cases} +2\pi K_{vco}R_PI_Pt & 0 < t < t_s \\ 2\Delta\varphi_{in} & t > t_s \end{cases} \tag{4}$$

$$\varphi_e(t) = 2\Delta\varphi_{in} - 2\pi K_{vco}R_PI_Pt \tag{5}$$

Substituting the above equations, the parameters in the simulation phase and phase to add additional output is achieved as follows.

$$\varphi_{out,ex} = \begin{cases} +15.03\times10^6 t & 0 < t < 0.132us \\ 2 & t > 0.132us \end{cases} \tag{6}$$

$$\varphi_e(t) = 2 - 15.03 \times 10^6 \times t \tag{7}$$

The lock system as well as the following equation is derived:

$$t = \frac{2\Delta\varphi_{in}}{2\pi K_{vco}I_PR_P} = 0.132\mu s \tag{8}$$

The results for the phase and phase to add additional outputs were compared with the simulation results in Fig. 6 (a) and (b) are plotted in Fig. 6 added to the phase difference between the reference [11] are compared (Fig. 6) shows that the major factor of stability, relationships and can provide highly accurate time-locked to a good show. It provided in relation to the project locking time 0/132us shows the simulation results of the time 0/13 us, which shows that the proposed method has high accuracy.

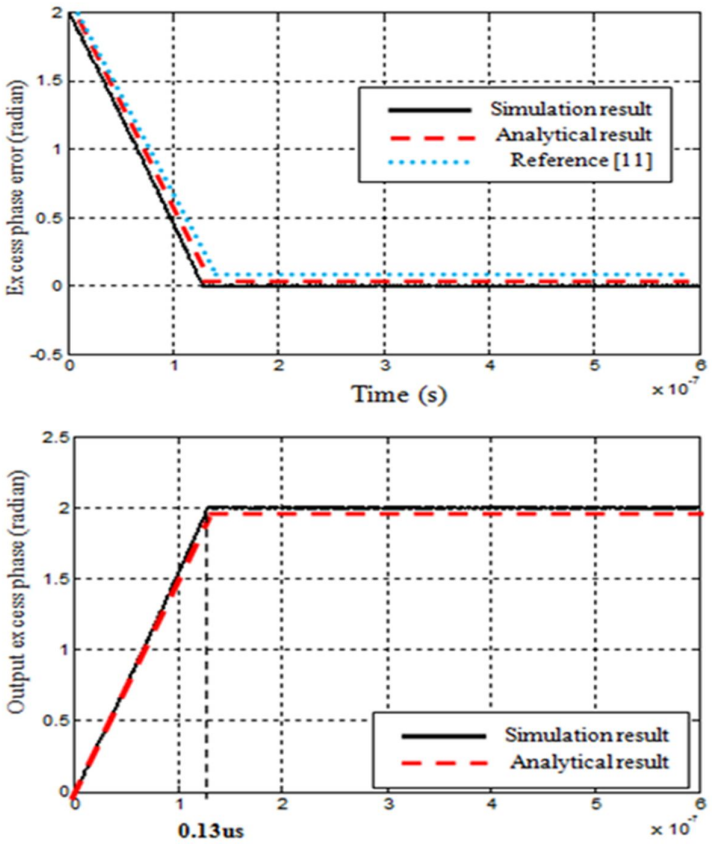


Figure 6. Comparison of analytical results with simulations of the stability factor is large in comparison with the reference [11] A. Add phase output: B. additional phase difference

Resistance and capacitance values have changed (Tab. 1) is observed, the stability factor is smaller, the error between the simulation and theoretical analysis are slightly higher. This is because the mined relations are established for large stability factor and the power goes to the smaller, of the system to oscillatory.

Table 1. Comparison of analytical results with simulation results for a lock of sustainability factors Settling time (us)

Simulation Result	Analytical Result	Stability Factor	Phase step (radian)
0/13	0/132	6000	1
0/0659	0/0663	4800	0/5
0/24	0/25	4000	1/3
0/13	0/15	800	0/8

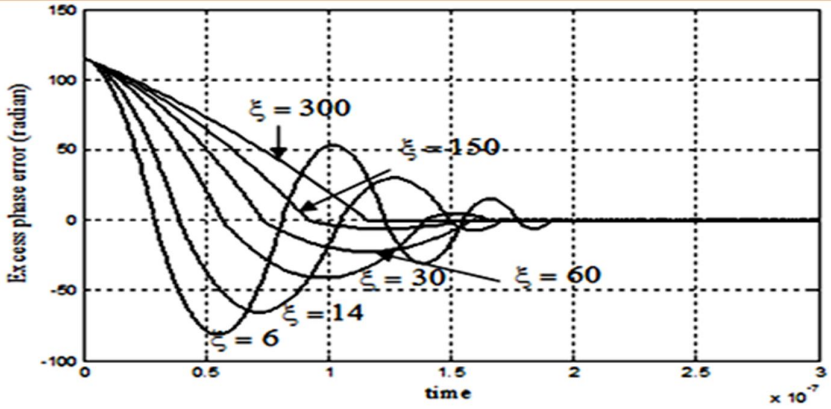


Figure 7. System response to step input of phase stability factors

Relations are obtained to analyze the transient behavior BBPLL input frequency step process.

4.2. Simulating Results in a Cycle Slipping

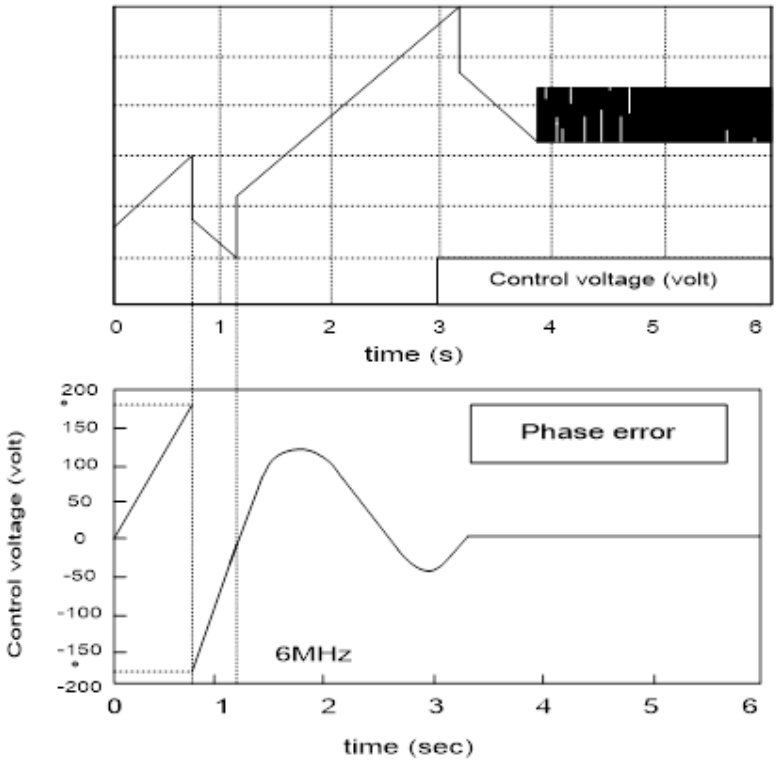


Figure 8. In response to step changes in voltage, frequency and phase control cycle slipping

Simulation Parameters:

$R_p = 500\Omega$ $I_p = 100\mu A$ $K_{vce} = 100MHziv$ $C_p = 500\,pf$ $\Delta f_{in} = 6MHz$

According to calculations, the design of the larger steps 4/76MHz is a cycle slipping. Therefore, we simulated the system for stepping 6 MHz (Tab. 2).

Table 2. Simulating results in a cycle slipping

Analysis of results	t'_s = 0.7us	t'_{rise} = 0.567us	$v'_{cot,max}$ = 0.146v	t'_p = 0.7us
Simulation	t'_s = 0.65us	t'_{rise} = 0.5us	$v'_{cot,max}$ = 0.14v	t'_p = 0.65us
[29]	t_s = 0.0912s	——	——	——

The above two equations show that the precision of the analytical method developed in the case BBPLL cycle slipping is too high. To test the above equation with control voltage got time intervals as follows:

$$v_{ut}(t) = \begin{cases} 0.05 + 2\times10^3 t & 0 \le 1 \le 0.079\,us \\ 0.04 + 2\times10^3 t & 0.079\,us \le 1 \le 0.107\,us \\ 0.06 + 2\times10^3 t & 0.107\,us \le 1 \le 0.187\,us \\ 0.023 + 2\times10^3 t & 0.187\,us \le 1 \le 0.224\,us \\ 0.073 + 2\times10^3 t & 0.224\,us \le 1 \le 0.353\,us \\ -2\times10^3 t & 0.353\,us \le 1 \le 0.4us \\ 0.093 + 2\times10^3 t & 0.4us \le 1 \le 0.65us \\ 0.12 & t \ge 0.65us \end{cases} \quad (9)$$

Compared with simulation results obtained from the equation in the form (8) is plotted.

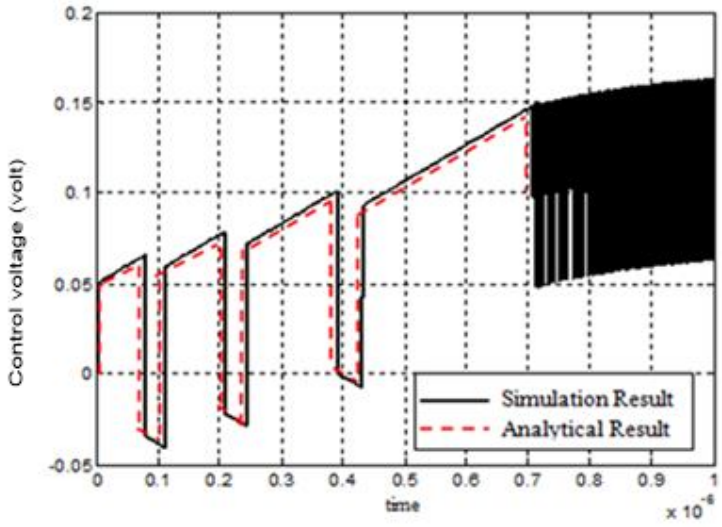


Figure 9. Comparison between the analytical results with the simulated response to a step input control voltage frequency cycle slipping

Fig. 8 shows that the proposed method has high accuracy. The form (8) can be seen in the size range $\pm 21_p R_p$ of the charging and discharging of the capacitor is higher jumps. In other words, the effect of the filter resistor voltage is greater than the capacitor voltage because this event is designed for large capacitors. To illustrate the general nature of the proposed method, a set of selected parameters which measure small capacitors to control the voltage in comparison with the simulation results plotted are shown below.

$R_p = 300\Omega \qquad I_p = 100\mu A \qquad K_{cv} = 100MHz \qquad C_r = 100\,pf \qquad \Delta f_{in} = 8MHz$

System design parameters of the entrance stairs7/5 MHz is a cycle slipping of the night, Pele 8 MHz have chosen. The equation for voltage control using the parameters listed above the following concepts to grasp.

$$v_{ut}(t) = \begin{cases} 0.05 + 2\times 10^{3} t & 0 \le 1 \le 0.079\ us \\ 0.03 + 2\times 10^{3} t & 0 \le t \le 0.043\ us \\ 0.01 + 1\times 10^{3} t & 0.043\ us \le t \le 0.o7\ us \\ 0.046 + 1\times 10^{3} t & 0.12\ us \le 1 \le 0.12\ us \\ 0.04 + 1\times 10^{3} t & 0.12\ us \le 1 \le 0.16\ us \\ 0.063 \times 1\times 10^{3} t & 0.16\ us \le 1 \le 0.35\ us \\ 0.093 + 2\times 10^{3} t & 0.4us \le 1 \le 0.43\ us \\ 0.16 & t \ge 0.43\ us \end{cases} \tag{10}$$

Equation is obtained. Fig. 9 is observed. The effect of voltage and resistance-voltage follow high-precision analytical simulations. Thus, in response to a step input frequency BBPLL transient behavior have been able to make clear and complete.

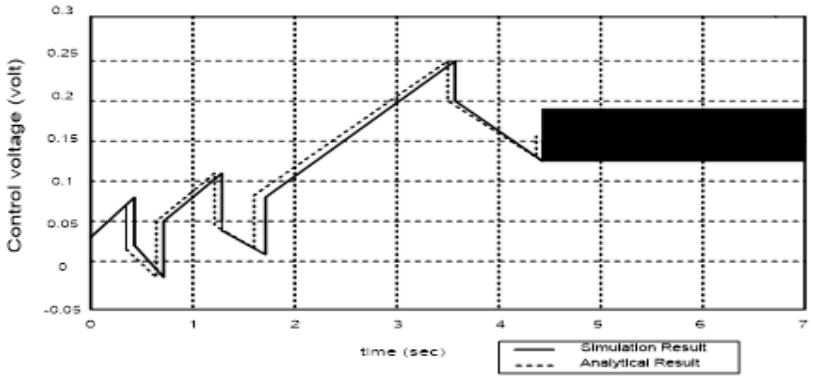


Figure 10. Comparison between the analytical results with the simulated response to a step input voltage controlled frequency filter capacitor.

The maximum transient voltage control in the experiment, the input bit rate of CDR circuits can be beneficial. In the next section, the effect of each of the design parameters on the transient characteristics we examine BBPLL.

4.2.1. Effect of Time Step on the Input Frequency Lock

In this section we examine the effect of input frequency on the time step size is considered a lock. As previously noted, in contrast to linear systems, nonlinear systems, the size of the input parameters affect the system. With increasing input size increases and decreases lock time is expected to reduce the waiting time to have a lock. In this part of the simulation we used parameters in the previous section. Again, write these parameters as follows:

$$R_p = 500\Omega \qquad I_p = 100\,\mu A \qquad K_{vco} = 100MHz/v \qquad C_p = 500\,pf$$

We noted above, the steps of design parameters than BBPLL 4/736 MHz of a cycle slipping phenomenon. The parameters of the stairs2/5 MHz, we start the simulation and analytical results with the simulation results we compare the lock time. The results in Figure 10 are occupied. As expected figure (10) shows that the larger the system the stairs4/736 MHz is a cycle slipping. For the case that the system does not see the cycle slipping Figure (10) shows that increasing the input step, the lock time is increased and the system runs the cycle slipping occurs, the position accuracy of the proposed method is also clearly seen in Fig. $\Delta f_{\text{in,slipping}} =$

$$\frac{40\times200\times300}{2} + \frac{1}{2}\sqrt{\frac{40\times200}{100\times10^{-12}}} \cong 4.736\text{MHz} \qquad (11)$$

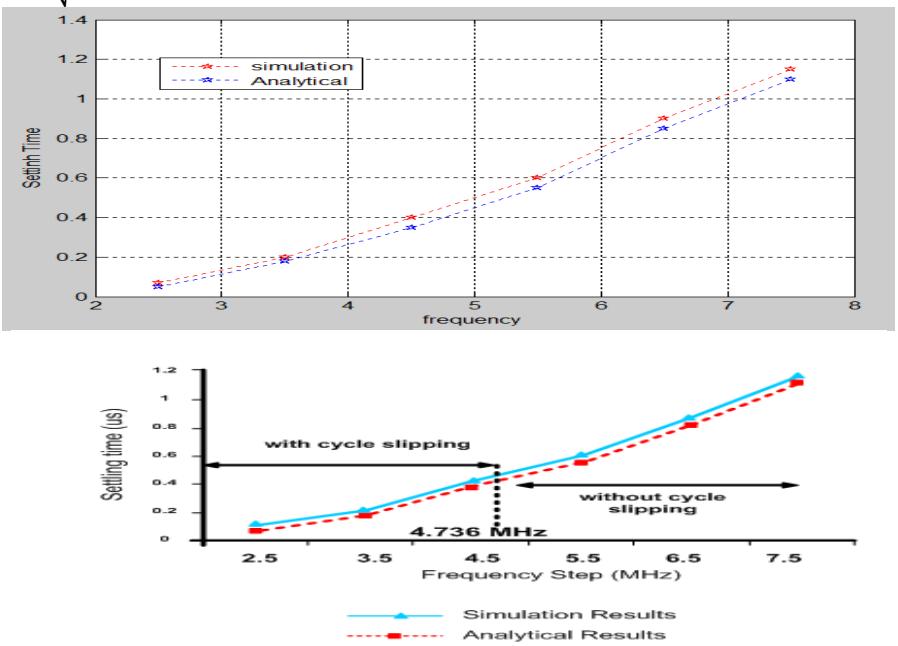


Figure 11. Comparison between analytical and simulation results of the time-locked to the input frequency step changes

4.2.2. Impact Resistant Lock Loop Filter Time

To investigate the effect of filter resistance on borrowed time lock and cycle slipping phenomenon that we have designed BBPLL with the following parameters.

$$R =_{p} = 400\Omega \qquad I_p = 100\mu A \qquad K_{vco} = 100MHz / v \qquad C_p = 300\,pf$$

The debt that we have entered a cycle slipping is affecting Pele. In this case, if the size of the filter resistance increases, we will see that the system is closer to the point in the cycle slipping out of step frequency. BBPLL with the design parameters with cycle slipping on stairs4.89 MHz is greater than the system we simulate the stairs 6 MHz Then we will see an increase in the resistance to the system at the frequency of the resistor 700, the next step will be another cycle slipping into. The comparison between analytical and simulation results in Fig. 11 are occupied. This form of resistance is observed in the system, the mode of cycle slipping out. The accuracy of the proposed method can clearly be seen in this figure. We can conclude that, with the remaining parameters of the design parameters can be configured into the system or cycle slipping into a cycle slipping can be prevented. The results show that the system can obtain greater strength in response to a step input frequency, the faster the cycle slipping phenomenon or not met. It should be noted that the great strength of the lock mode, would undermine the stability of the system.

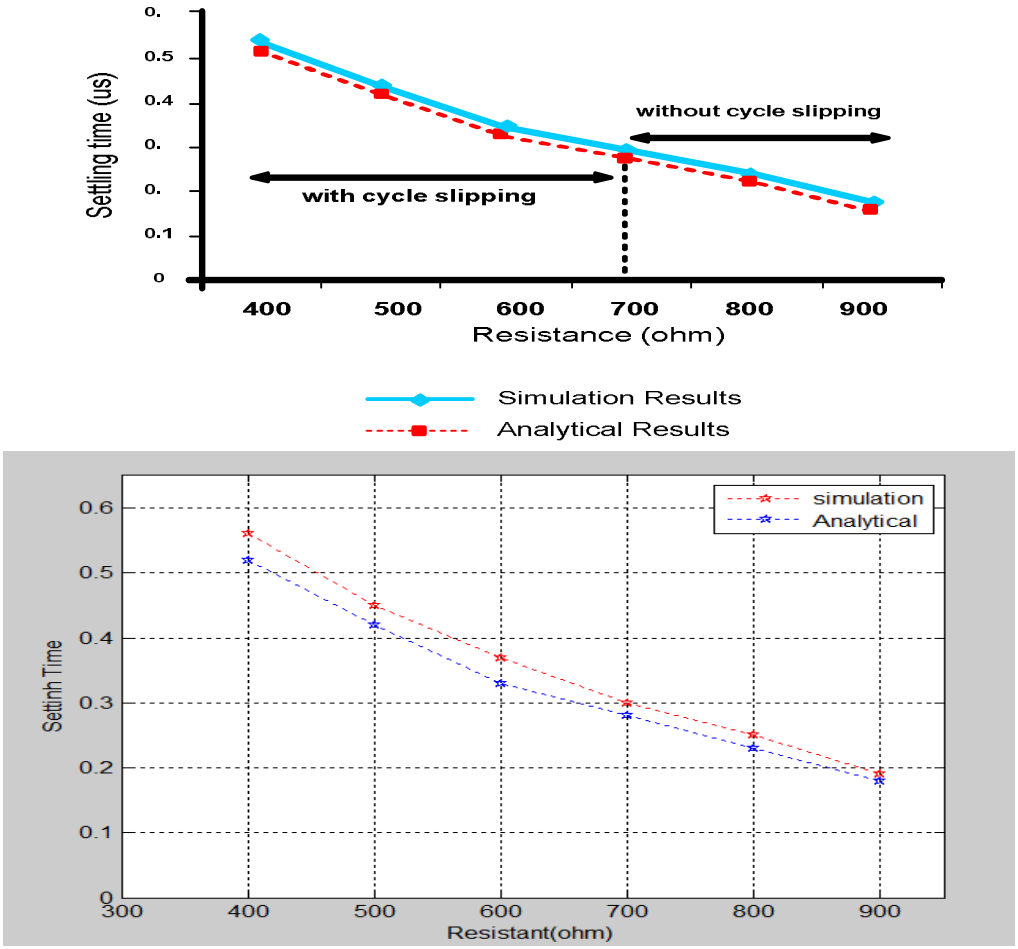


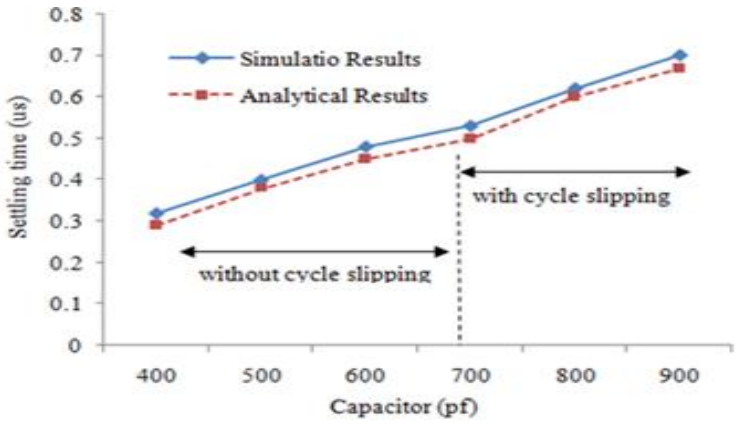
Figure 12. Comparison between analytical and simulation results lock resistant to change filter

4.2.3. Effect of Time Locked Loop Filter Capacitor

As in the previous section, the effect of loop filter capacitor on the lock and cycle slipping phenomenon considered.

$$R_r = 400\Omega \qquad I_p = 100\mu A \qquad K_{vcv} = 100MHz / v \qquad C_p = 400\,pf$$

Suppose that System design parameters set out below have been designed to be larger than the system design parameters of the stairs 4/5MHz with cycle slipping is, the system will simulate the steps 4 MHz, as the cycle slipping not experience if you increase the size of the loop filter capacitor. We shall see that the system is going in the same direction as the step frequency cycle slipping phenomenon to experience.



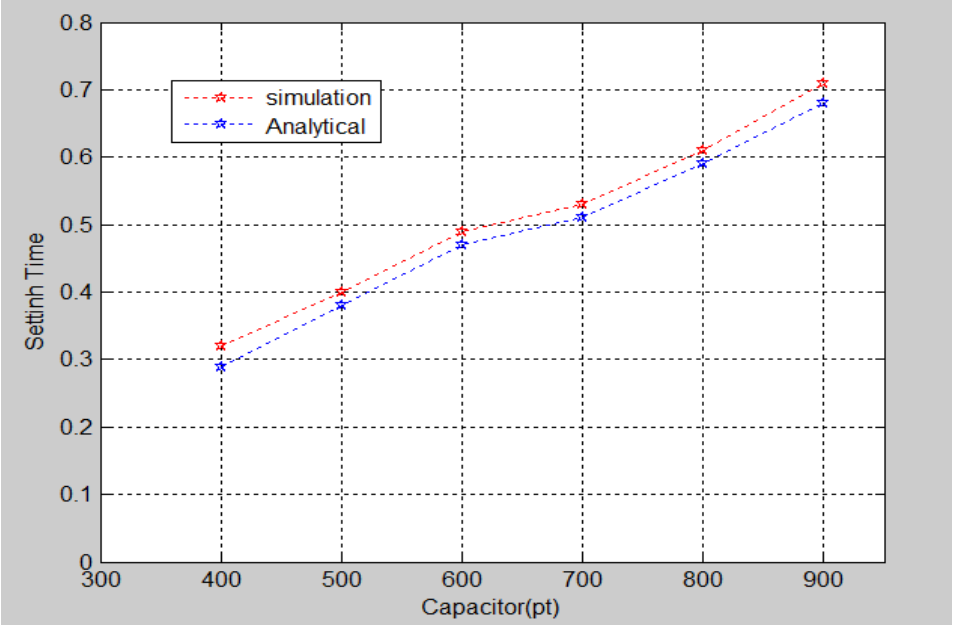


Figure 13. Comparison between analytical results and simulated lock time to change the filter capacitor

In the simulations performed, the filter capacitor 900 pf will enhance the analytical results with simulation results we compare the lock time. The results in Fig. 12 are occupied. Fig. 12 is seen in a larger capacitance700 pf cycles slipping is entered undesirable phenomenon. The results can be found or a large capacitor, the larger will be locked during the transient response to input or frequency will be associated with the phenomenon of cycle slipping. The remarkable thing here is that the design for a sustainable BBPLL, size large capacitance, so we can conclude that most of the design cycle slipping phenomenon exists.

4.2.4. Effect of time of maximum pump flow control voltage

Another circuit parameters that affect the maximum value of voltage control is also effective in the development cycle slipping phenomenon, the pumping time. The orbital parameters of the circuit parameters that affect the transient time, here we have examined the effect of some of them. For the simulation we used the following parameter sets.

$R_p 400\Omega \qquad I_p = 90\mu A \qquad K_{vco} = 100MHz/v \qquad C_P = 400\,pf$

The system parameters in larger steps 4/17 MHz with cycle slipping causes the system to cycle slipping on stairs 5MHz simulations we observe. Then again, each time increasing the amount of current at a frequency simulation steps to do the same. Analytical results for the maximum control voltage is compared with the simulation results in Fig. 13 are derived. In this figure we see that larger values of the maximum voltage is reduced as a result of Fig. 13 is found, the system does not see the cycle slipping, will experience greater maximum voltage

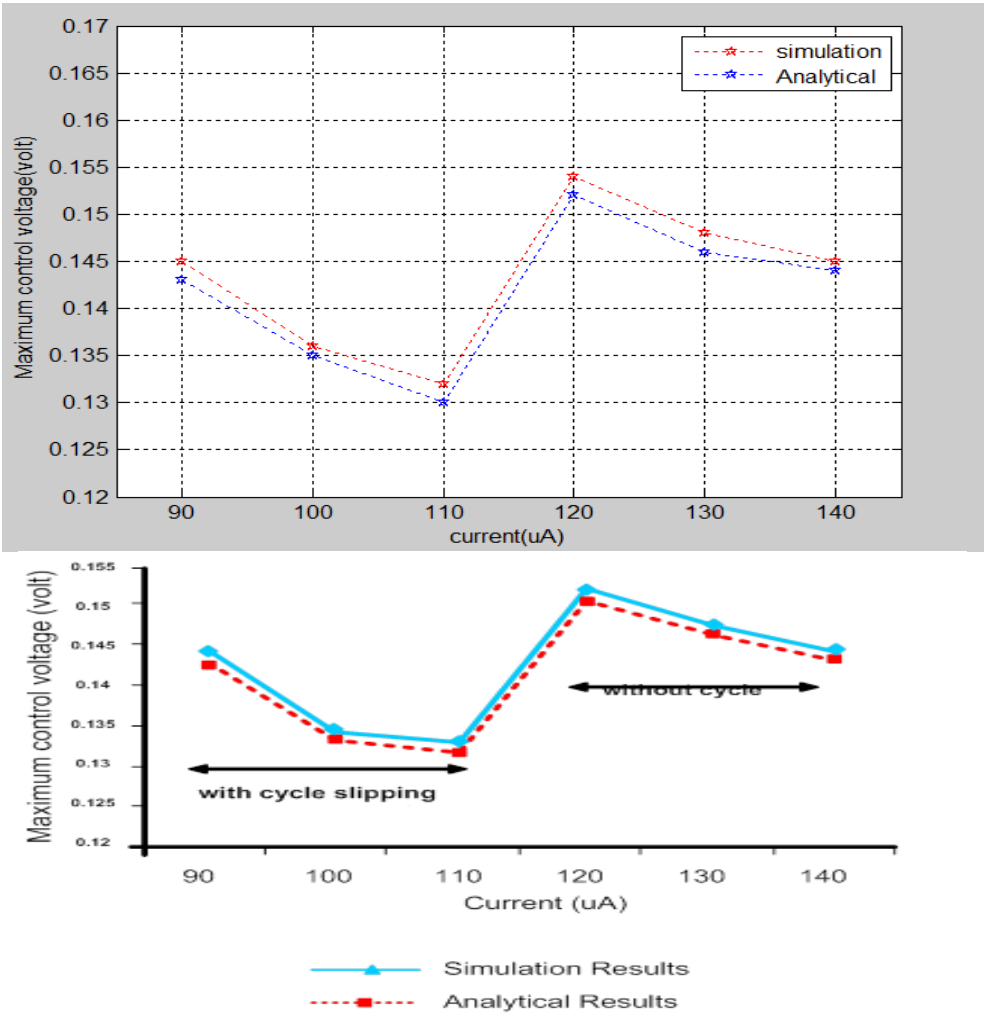


Figure 14. Comparison of analytical and simulated maximum flow of pump control voltage to the Times

So far, the accuracy of the extracted relations extracted carefully examined and the effect of design parameters on the characteristics of each setting when we have analyzed germ after considering the boom in the mining BBPLL design process (Fig. 14).

5. Conclusion

The results can be downloaded. The proposed methods for modeling the phase detector and the differential equation are obtained by the simulation for acceptable accuracy. The mathematical model for the system response to a step input frequency is extracted, passing the time with all the features that have been extracted, they are well described system behavior.

Designed to predict the stability and speed BBPLL can be helpful in optimizing the design. Evaluation of system response to a step input phase can be a criterion for the design of more efficient and specific BBPLL ratio a / b can BBPLL criterion to predict the peak of the transfer function in the frequency domain is chiter. This is much larger than the amount of the transfer function chitter peak will be lower. This fact may be related to mutations in the areas of the peaks in the frequency domain and time of receipt of the concepts of linear control. Painful and time-consuming operation in BBPLL locks are designed for multiple inputs with different bit-rate, very important. Analysis of the evaluation system for step input frequency can meet the requirements of the system.

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