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Single Miller Capacitor Frequency Compensation on Three Stage Amplifier for Large Capacitive Load

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ABSTRACT

This paper presents the analysis of single Miller compensation scheme which is used in three-stage CMOS operational amplifiers. single Miller compensation capacitor in three-stage amplifiers can significantly reduce the total capacitor value, and therefore, the overall area of the amplifiers without influencing their stability. In this paper we reviewed achieving high stability in addition to wide bandwidth, and comparing to all the structures have been presented, it has higher stability and bandwidth. The value of the compensation capacitor is also reduces significantly. There for, firstly we review the amplifier structure and finally, bring the Simulation results and proposed Dimensions. conducted Simulations in this paper was on 0.25µm for (25-kΩ//120Pf) large load.
KEYWORDS: Stability, frequency compensation, three stage amplifier, single miller compensation

1. INTRODUCTION

Operational amplifier in negative feedback arrangement, used widely in analog circuits such as regulators, filters and the data converts for buffering and filtering [1]. Regarding to the minimum number of transistors, one stage operational amplifiers have the best frequency response, and have higher speed comparing to multi stage amplifiers. It may be able to eliminate the effect of non-linear open-loop system (in closed loop configuration) sufficiently, but due to the DC open-loop gain can be achieved in these structures, especially in new technologies, it is not noticeable. To solve this problem, in most cases, two and three stage Op Amp are used for frequency compensation [2]. Three stage amplifiers are highly desirable , due to their high voltage gain. Unfortunately, from the point of view of stability and bandwidth they are low. So achieving high stability in an appropriate bandwidth can be most efficiently. For large capacitive loads of up to three categories of amplifiers it is inevitable. Therefore, these amplifiers are needed to robust high frequency compensation scheme to have good stability of the closed-loop arrangement. Among the techniques introduced for driving of large capacitive loads in three stage amplifier, Single miller capacitor Compensation amplifier, has several advantages due to using one compensation capacitor instead of two, such as: Low overall area, greater bandwidth, greater stability and smaller compensation capacitor. In this paper, the design was based on achieving a wide bandwidth in a high phase margin and the compensation capacitor value is reduced as much as possible. Achieving to this aim, firstly review different three stage amplifier with large capacitor load and then, the structure of SMC. Finally, bring the result of Simulation and the proposed Dimensions of transistors.

2. Background and pervious work

Among the Frequency Compensation schemes, Nested Miller Compensation (NMC) are not suitable for large capacitive loads. Because Its bandwidth is severely limited due to stage increasing[3]. The size of compensation capacitor also increase proportionally with the load capacitor . This drawback led to other compensation schemes such as Multipath Nested Miller Compensation (MNMC) [3]. This scheme introduces a feedforward path for high frequencies that improves the bandwidth of the overall amplifier by pole-zero cancellation within the passband. passband. Stability of the NMC is improved by removing the right half-plane (RHP) zero. To this end, phase compensation schemes such as nested Gm-c compensation (NGCC) [4] and NMC with feedforward transconductance stage and nulling resistor (NMCFNR) [5] have been reported. Small compensation capacitor helps to stability of much higher bandwidth. All of the above compensation techniques ,use miller capacitor whose size depend on the size of load capacitor. For large loads, the size of the tend to increase Miller capacitors. For Reducing these problems, and increasing bandwidth we use some schemes such as: No Capacitor FeedForward compensation(NCFF) [6] and Active Feedback Frequency Compensation (AFFC) [7]. NCFF is based on pole-zero cancellation at high frequencies resulting in higher bandwidth and faster settling time. In AFFC we use an active capacitor which reduce the size of the

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compensation capacitor. There are another compensation schemes on three stage amplifiers, for example Damping Factor Control Frequency Compensation (DFCFC) [8] which uses The damping control block on pole complex position, or Dual LOOP parallel Compensation (DLPC) [9] but none of noted technique are suitable for driving a large capacitor loads.

3. Single Miller capacitor compensation Amplifier (SMC)

In most three stage amplifier structures were used two compensation capacitor to driving a large capacitor loads. But the Compensation presented in this section, only a small capacitors used for three stage amplifiers. In amplifiers with a large capacitive load, last stage poles are usually very small and it is so near to the dominant pole which is located on the first stage, and should be lower it's effect by One of the most common compensation. In Usual pole spliting has been used. In figure (1) you can see the structure of SMC amplifier.

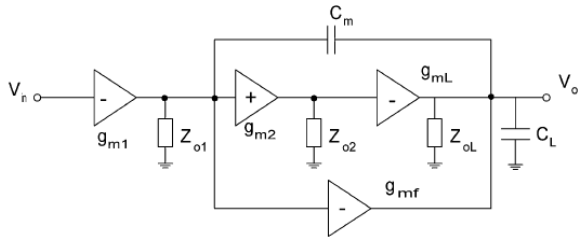

Figure1: *Topology of single Miller capacitor compensation amplifier (SMC)*

A larger bandwidth can be obtained by using only one capacitor for compensation instead of two. The structure has three gain stages with only one compensation capacitor. It has an additional transconductance stage (gmf) from the output of the first stage to the final output. This forms a push-pull stage at the output that helps in improving the transient response of the amplifier. a single Miller compensation capacitor(cm) is used to split the first pole(p1) and the third pole (p3). The position of the second nondominant pole(p2) is dictated by the gain of the second stage, which decides the stability of the amplifier[10].

3.1.Small-Signal Analysis

Small-signal analysis is carriedout with the following assumptions.

1.The gain of all stages are much greater than 1.

2. The Parasitic capacitances C_{P1} ,C_{P2} and C_{PL} are much smaller than the Miller capacitor C_m and load capacitor C_L .

3. The transconductance of the feedforward stage, g_{mf}, is equal to that of the third gain stage, g_{mL}.

The transfer function is given by (1):

(1)

$$AV_{(SMC)}=\frac{VO(s)}{Vin(s)}=\frac{Adc(1+s\frac{C_{p2}g_{mf}-C_m g_{o2}}{g_{m2}g_{mL}}-s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}})}{(1+\frac{s}{p_{-3dB}})(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}})}$$

$$\approx\frac{(1+s\frac{C_{p2}g_{mf}-C_m g_{o2}}{g_{m2}g_{mL}}-s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}})}{\frac{s}{GBW}(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}})}$$

Where $AV_{(SMC)}(0)=A_{dc}=(g_{m1}g_{m2}g_{mL}/g_{o1}g_{o2}g_L)$ is the dc gain of the amplifier, and $P_{3-dB}=(g_{o1}g_{o2}g_L/g_{m2}g_{mL}C_m)$ is the dominant pole of the amplifier. Hence, the gain-bandwidth product is given

by $GBW = A_{dc} \cdot p_{3-dB} = g_{m1} / C_m$. From the transfer function, the amplifier has two nondominant poles and two zeros.

3.2. stability analysis

The stability condition of the SMC amplifier can be determined by analyzing the closed-loop transfer function with a unity-gain feedback configuration. Since the zeros are located at a higher frequency, they are neglected. The closed-loop transfer function is

$$A_{cl(SMC)} \cong \frac{1}{1+(\frac{sC_m}{g_{m1}})(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}}+s^2\frac{C_{P2}C_L}{g_{m2}g_{mL}})} \quad (2)$$

$$= \frac{1}{a_0 s^3 + a_1 s^2 + a_2 s + a_3}$$

which can be written as:

$$a_0 = \frac{C_{p2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \quad (3)$$

$$a_1 = \frac{g_{o2}C_L C_m}{g_{m1}g_{m2}g_{mL}}$$

$$a_2 = \frac{C_m}{g_{m1}}$$

$$a_3 = 1$$

Amplifier stability derived from closed-loop transfer function (2) ,which the order of the numerator is less than than that of the denominator. so, writing down closed loop transfer function and applying the Routh–Hurwitz stability criterion on the characteristic

equation of transfer function (4), it yields

$$a_1 a_2 - a_0 a_3 > 0$$

$$\Rightarrow \frac{g_{o2}}{c_{p2}} > \frac{g_{m1}}{c_m} = GBW \quad (4)$$

If and only if condition (4) is satisfied, the system is unconditionally stable. For large capacitive loads, the stability analysis of the amplifier can be done using the separate pole approach Assuming that the zeros of the amplifier are located at higher frequencies and hence can be neglected, the nondominant poles of the amplifier are calculated as follows.

$$P_2 = (G_{meff} / C_L) \quad (5)$$

$$P_3 = (g_{o2} / C_{p2}) - (G_{meff} / C_L) \quad (6)$$

$$G_{meff} = (g_{m2}g_{mL} / g_{o2}) \quad (7)$$

The value of the compensation capacitor become $C_m = \frac{1}{A_{V2}}(2\frac{g_{m1}}{g_{mL}}C_L)$. This represents a compensation capacitor is very small thus,it can be seen that by suitable choice of the second-stage gain ; $A_{v2} = (g_{m2} / g_{o2})$ ، The value of the compensation capacitor can be reduced. Note that, Zeros of the transfer function depends on the compensation capacitor if the value of this capacitor is too small, zeros are placed at very high frequencies[10].

The phase margin is calculated as follows:

$$PM = 180 - \tan^{-1}(\frac{GBW}{P_1}) - \tan^{-1}(\frac{GBW}{P_2}) - \tan^{-1}(\frac{GBW}{p_3}).$$

3. 3. Slew Rate and Settling Time

The transient response of the amplifier is comprised of the slewing and settling behavior of the amplifier in closed-loop condition. The slew rate of the amplifier depends on the size of the compensation capacitor. The significant increase in the slew rate of SMC as compared to that of NMC under the same power constraint is due to the reduction in the size of the compensation capacitor. The Settling time of the amplifier has two components of Small signal and large signal time. Bandwidth achieved in SMC structure, obtained by sacrificing absence of doublet in the passband of the amplifier, There is no trouble in small signal time. This part influenced by bandwidth. In addition the time of large signal is very low regarding to the small amount of the compensation capacitor and Slew Rate finally do not influenced by the compensation capacitor.

3.4. Design Considerations and Circuit Implementation

A judicious distribution of gain among the three stages is one of the most important considerations in the design of these amplifiers $> 100dB$, the gain is distributed such that $A_{v1} \square A_{v2} > A_{v3}$. This results in the second and third pole of the amplifier being located at higher frequencies due to the high output conductance of the second and third stages. This roughly results in a single-pole system. In order to achieve this, the first stage uses a folded cascode topology to enhance the output impedance. A moderate gain at the second stage helps in reducing the required compensation capacitor to a great extent. For example, a 100-dB gain from three stages can be distributed as 60, 30, and 10 dB for the first, second, and third stages, respectively. thus A_{v2} =30dB resulting in a reduction of the required $_{cm}$ by a factor of $2 \times 30 = 60$ compared to that of NMC while maintaining stability. The circuit implementations of the SMC amplifier is shown in Figs (2). transistors M_1-M_8 form the first gain stage.. The second gain stage of the amplifier is comprised of transistors M_9-$M_{12.}$ The output stage is comprised of a feedforward Stage $_{gmf}$ and the third gain stage gml forming a push-pull stage. The third gain stage is realized by transistor $_{M13,}$ whereas the feedforward stage is realized by transistor $_{M14.}$ The gate–drain capacitance of transistor $_{M13}$ forms an additional Miller capacitor between the second and third stages. Since the parasitic capacitor value and the gain of the third stage are small, it is neglected.

4 . Simulation Results

Circuit-level simulation results are obtained with 0.25 μm BSIM3 2.5 V models using HSPICE. All the results above are with a 25kΩ //120-pF load. In this paper an attempt has been done to design compensation capacitor as small as possible. the value of the Miller capacitor is 3pf. Table (1) contains the proposed dimension of transistors which Simulations have been performed based on them. In SMC our target was reaching to High phase margin in a wide bandwidth. in addition, they should have High DC gain, and finally we reach to 76º phase margin in a 6.3MHZ bandwidth, which is optimum and comparing to previous models is much more better. In figure (3) you can see, Simulation of frequency response of SMC open loop amplifier. Among The parameters of closed loop we can mentioned settling time slew rate. Both of them are Important parameters for operational amplifiers and achieved from Transient closed-loop system status. Since this design have higher bandwidth, it have higher speed and better settling time and slew rate comparing to pervious structure. In figure (4) you can see closed-loop simulation of designed structures. with the 1.5-V step input, there is an overshoot for the up-going signal. For the low voltage and the high voltage, the operating points of the transistors in the circuit are different, which means that the effective pole, zero locations of the amplifier are different for rising and falling signals. This is the reason why overshoot appears for up-going signal, and not for down-going signal. The 0.1% settling time $_{is}$ considered. in table (2), a comparison between new designed and previous models has been done, then we could prove the superiority of above design.

***Table 1**: transistors proposed dimensions.*

TRANSISTOR	SMC
Mb1	2*(1.9/0.5)
Mb2	8*(1.9/0.5)
M1,2	8*(2.8/0.3)
M3,4	6*(0.9/0.5)
M5,6	2*(0.9/0.5)
M7,8	6*(2.8/0.966)
M9	6*(3.28/0.3)
M10,11	2*(2.5/0.48)
M12	6*(1.9/0.3)
M13	2*(8/0.32)
M14	10*(3/0.2)

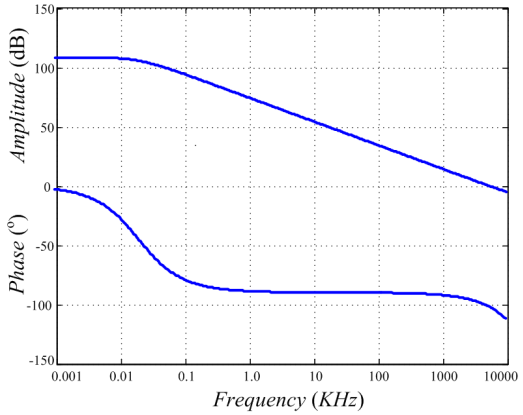

***Figure3**: opamp loop-gain frequency response of SMC*

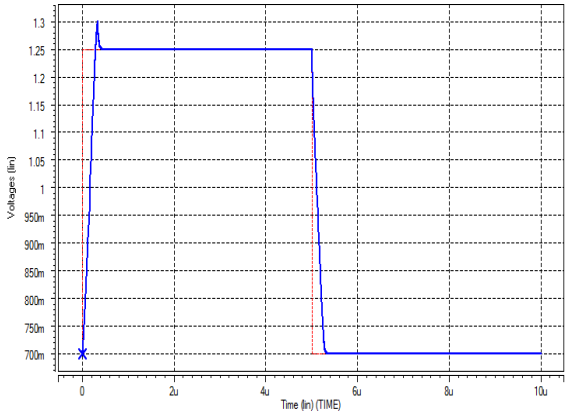

***Figure4:** opamp close- loop frequency response of SMC*

5 . Conclusion

In this paper, single miller capacitor frequency compensation was presented on three stages amplifiers, and comparing to previous structures have better bandwidth and phase margin. In addition, Compensation capacitor value is decreased significantly. Regarding to settling time and slew rate of this system have appropriate Values.

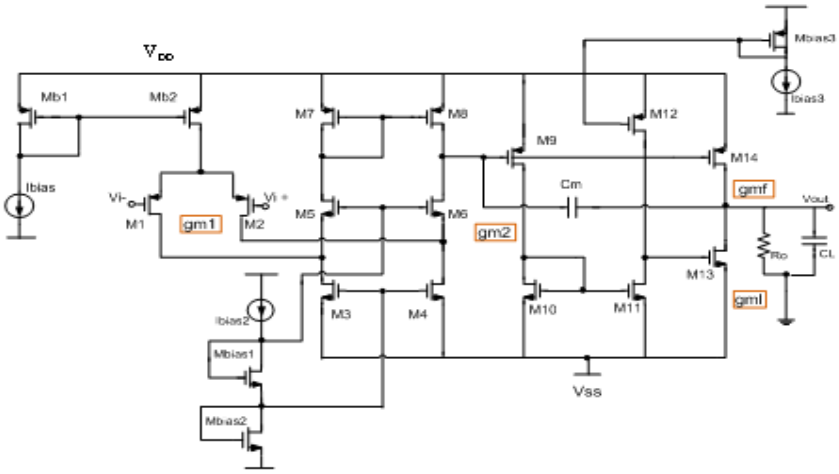

***Figure2**: Schematic of the SMC amplifier.*

Table2: *A comparison between multi-stage amplifiers with large capacitive load.*

PARAMETER	NMC [7]	DFCFC [8]	AFFC [7]	DLPC [9]	SMC [10]	SMC THIS WORK
Load PF/kΩ	120/25	120/25	120/25	120/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100
GBW(MHZ)	0.4	2.6	4.5	7	4.6	6.3
Phase margin	61	43	65	46	58	76
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	C_{m1}=3 C_{m2}=7	C_{m1}=4.8 C_{m2}=2.5	C_m=7 one	C_m=3 one
SR+(V/μS) SR-(V/ μS)	0.15 0.13	1.32 1.27	0.78 2.20	2.2 4.4	3.28 1.31	1.6 2.2
+1% TS(μS) -1%TS(μS)	4.9 4.7	0.96 1.37	0.42 0.85	0.315 0.68	0.53 0.4	0.426 0.35
Technology	0.8 μm CMOS	0.8 μm CMOS	0.8 μm CMOS	0.6 μm CMOS	0.5 μm CMOS	0.25 μm CMOS

REFERENCES

[1] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2000.

[2] H. Aminzadeh, M.Danaie,R.Lotfi "Design of high-speed two-stage cascode-compensated operational amplifiers based on settling time and open-loop parameters "Elsevier,vlsi journal, 2008.

[3] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dBerational amplifier with multipath nested Miller compensation structure," *IEEE J. olid-State Circuits*, vol. 27, no. 12, pp. 1709–1717,Dec. 1992.

[4] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G -C compensation," *IEEE J.Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[5] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low power CMOS design," *IEEE Trans. Circuits Sys. II*, vol. 48, no. 4, pp.388–394, Apr. 2001.

[6] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.

[7] H. Lee and P. K. T. Mok, "Active-feedback frequency compensation technique for low power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.

[8] K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three stage large capacitive load amplifier with damping-factor control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.

[9] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.

[10] X. Fan, C. Mishra, and E. Sanchez-Sinencio, 'Single Miller Capacitor Frequency Compensation Technique for Low-power Multistage Amplifiers,' IEEE J. Solid-State Circuits, vol. 40, no. 3, pp. 584-592,Mar. 2005.