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A New Low Power Full Adder Cell Based On Carbon Nanotube Field Effect Transistors

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ABSTRACT

Full adders are the most important cells in the logic and mathematics unit. In this paper, we present a new low power full adder cell designs using carbon nanotube field effect transistors (CNTFETs). In this design we have 26 carbon nanotube field effect transistors so, that we have achieved an improvement in the output parameters. Simulations were carried out using HSPICE based on the CNTFET model with 0.9V V_{DD}. The results of power, Delay and power delay product show that this design is more optimal than the previous works.
KEYWORDS: CNTFET; Low power full adder; Carbon nanotubes; Field effect transistors.

INTRODUCTION

Carbon is one of the amazing elements in the nature [1]. Carbon nanotubes are one of the forms of carbon structures which are made of the rolled graphite sheets and they are in two types: single wall and multi wall [2].

CNTs given the angle between the atoms and the Arrangements of carbon atoms together are divided into Armchair, Chiral and Zigzag categories [2].

Creation the carbon nanotube field effect transistors or CNTFETs is because of the using carbon nanotubes in the design and manufacture of electronic switches. Many problems have been introduced because of the limitations of MOSFET technology [3]. We have achieved the CMOS physical limitations by extenuation the size of cmos circuits; molecular devices are suitable hopeful alternatives to the existing silicon technology [4]. The unique properties of CNT such as high volubility of electrons, high Ion/Ioff ratio and their unique one dimensional band structure that suppresses back scattering and near ballistic or ballistic operation has made it as a potential successor to silicon MOSFETs[5].

Carbon Nano Tubes Field Effect Transistors (CNTFETs) have additional scalability and less scale in comparison with MOSFET transistors and this feature make them suitable for displacing of this technology [3]. These transistors are made of carbon nanotubes as their channel. In this paper we present a new full adder cell with using these features of carbon nanotubes to optimize the output parameters and also achieve the new design of full adder cell.

CNTFETs made by single-walled carbon nanotubes which have semiconducting properties and Single-walled carbon nanotubes formed with hollow cylinder of carbon [4]. Conductivity of nanotubes is specifying with a pair of integers that called chirality vector (m, n).

Depending on the value of m and n, the nanotubes are divided into three categories: armchair, Chiral and zigzag [5].

The diameter of the nanotubes is an important parameter of CNTs which calculated by Equation 1.

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{m^2 + n^2 + mn} \qquad \text{eq1}$$

By using this equation we can calculate the appropriate value for the diameter of the nanotube.

Another advantage of CNTs is that the threshold voltage can changed by changing the carbon nanotube diameter. (eq2)

$$V_{th} = \frac{0.42}{D_{CNT}(nm)}\ V \qquad \text{eq2}$$

Carbon nanotube field effect transistors are divided into two types of N and P.

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CNFETs work similar to traditional silicon transistors. Different types of CNFETs have been implemented. One of these types is Schottky Barrier CNTEF that called SB-CNFETs. SB-CNTFETs are made with a semiconducting nanotube and two metallic contacts operating as source and drain; so they have Schottky Barrier at the metal nanotube connection. In SB-CNTFETs By shifting the barrier height at the metal- semiconductor junction, gate adjusts the connection of carriers in the nanotube. MOSFET-like CNFETs are another type of CNFETs that exhibit unipolar actions [6].

CNFETs has an effective feature that It will ease the designing of logic circuits and increase the performance of circuit on the other hand, the threshold voltage is related to the inverse of the nanotube's diameter [6].

In this paper, we present an optimized full adder cell design with using CNTFETs.

The scientific contributions of this paper are:

1) Using the carbon nanotube field effect transistors in this design.

2) Using only CNTFETs without resistor and capacitor elements in this full adder cell design.

3) Decrease the number of transistors and size of chip in comparison to previous works.

PREVIOUS WORKS

Many designs of full adder circuits have been presented. One of these designs was hybrid that presented with using 24 CMOS transistors [7]. Other Full adder cell designs are based on multiplexers [8,9], The Full Adder that presented in [9] implements with minimum number of transistors. The designers have presented many full adder cell circuits based on majority functions [10–14]. In this paper we will compare the result of our new proposed designs with 4 recent presented Full adders. One of these full adders has 7 capacitors which implements output parameters by equation 3. (Fig.1)[11].

In this design $\overline{C_{out}}$ and $\overline{SUM}$ have implemented by using majority-not function.

$$\text{Majority}(A,B,C) = AB + AC + BC = C_{out} \quad \text{eq3}$$

$$SUM = Maj(A, B, \overline{C_{out}}, \overline{C_{out}})$$

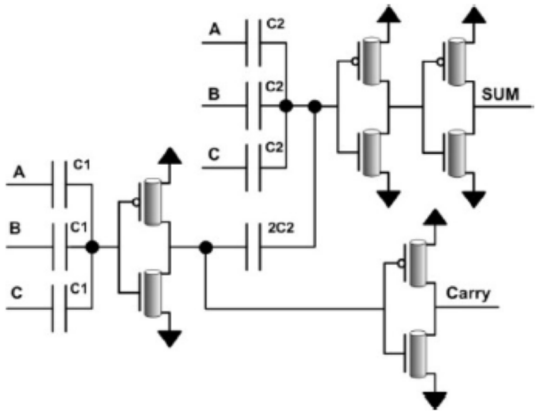

Figure 1. Full adder1 [11]

Next design reduced the number of the capacitors and the circuit parameters were better than previous designs (Fig.2)[13]. Another full adder cell presented with using 10 transistors and 8 capacitors (Fig.3)[15]. This full adder cell was based on the minority function.

In this circuits they used a NOT function to reach the full adder outputs because $\overline{SUM}$ and $\overline{C_{out}}$ was implemented.

In the last design two circuits were implemented. In the first one used 42 transistors and 5 pull up resistance but the power parameter of this design was more than pervious works so in the second one the outputs were optimized by using transistors instead of resistances (Fig.4)[16].

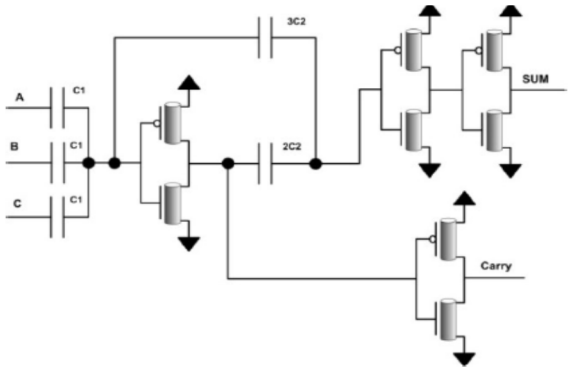

Figure 2. Full Adder 2

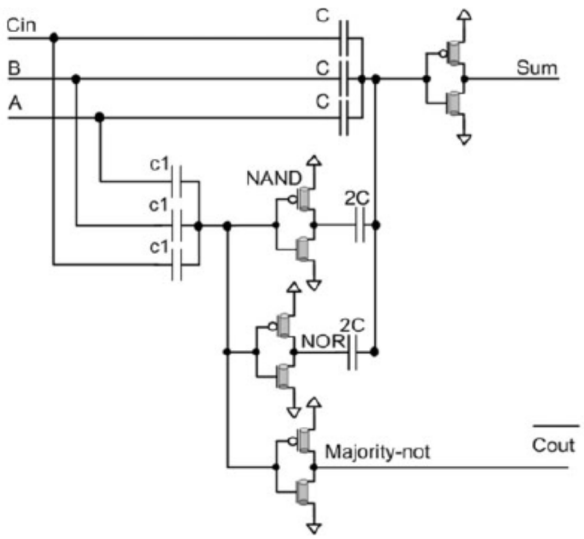

Figure 3. Full Adder3

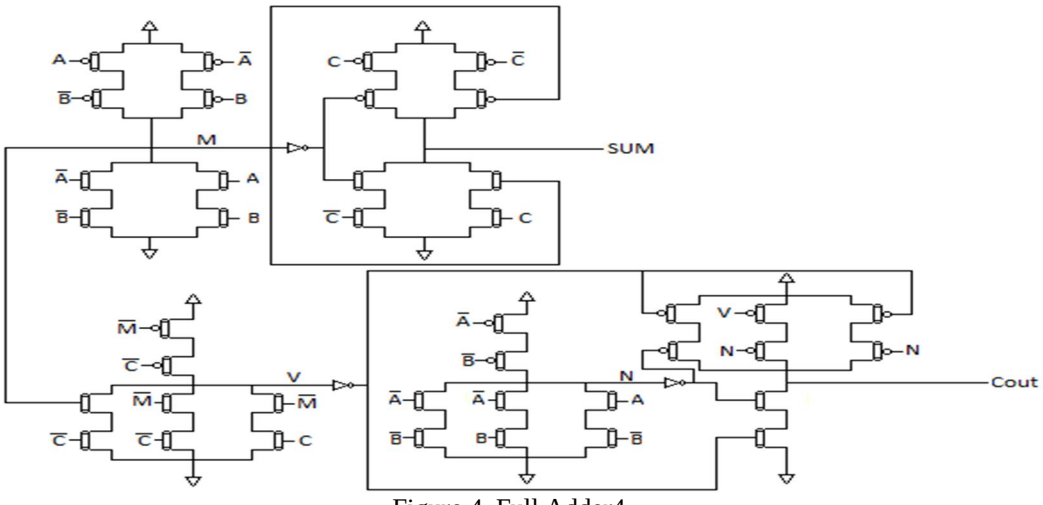

Figure 4. Full Adder4

In the last full adder cell designs $\overline{SUM}$ and $\overline{C_{out}}$ was implemented and they should used a NOT function to achieve the full adder outputs.

PROPOSED FULL ADDER

In this paper, we presented a new optimal full adder cell. In this design (figure5) we used 26 carbon nanotube field effect transistors, we have achieved a significant improvement in our output parameters. Fig 6-8 shows this simulation results.

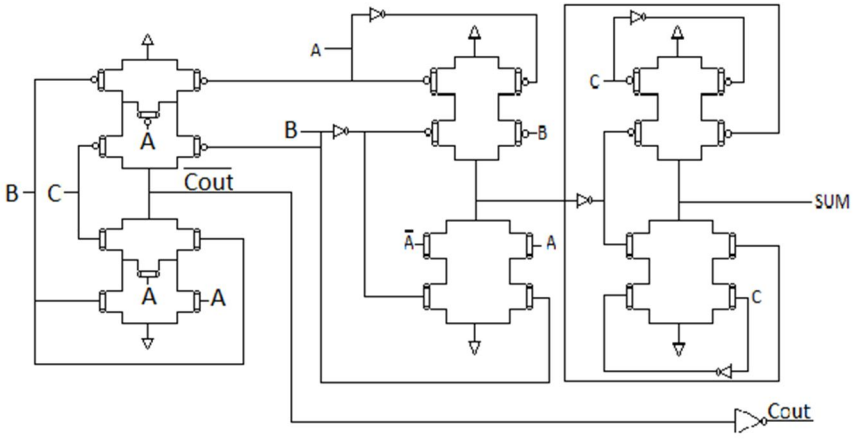

Figure 5. Proposed design

The outputs of this full adder cell are completely full swing as shown in Figure 6. In this figure the A, B, Cin inputs and sum, Cout outputs are illustrated in order from top to bottom (Figure 6).

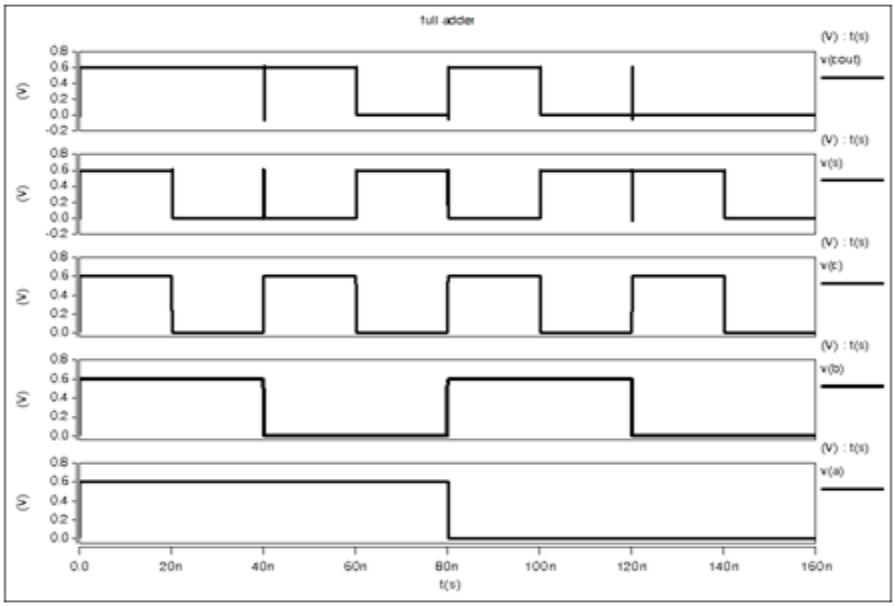

Figure 6**. S**imulation results (A, B, Cin, Sum, Cout)

The simulation result of PDP, delay and power parameters is showed in table 1.

	Power	Delay	PDP
Full adder-1[7]	5.23E-07	7.97E-11	4.17E-17
Full adder-2[8]	4.71E-07	8.82E-11	4.15E-17
Full adder-3[9]	7.12E-07	7.51E-11	5.35E-17
Full adder-4[16]	1.35E-08	3.45E-11	4.663E-19
Proposed Design	6.45E-09	3.22E-11	1.85E-19

Table 1. Simulation results (A, B, Cin, Sum, Cout)

In this design we decrease the number of transistors. The power and delay of our proposed design are less than previous designs because of using the lower number of transistors and less size in comparison to the previous works. In this design we decrease the number of transistors Figures 7 to 9 compared the output results with previous designs. Another cause of this improvement is using only CNTFETs without resistor and capacitor elements in this full adder cell design.

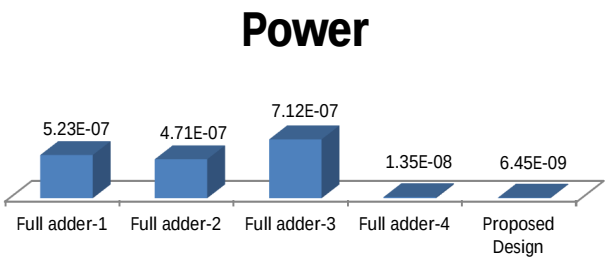

Figure 7. Power results

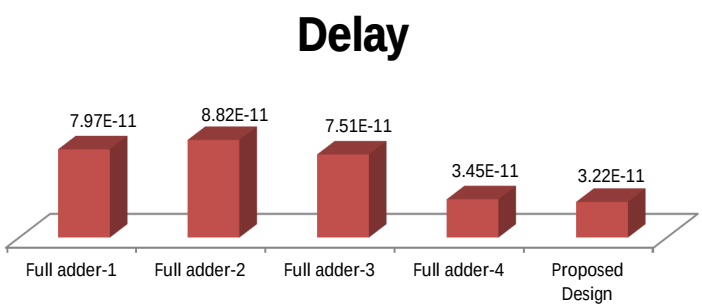

Figure **8.** Delay results

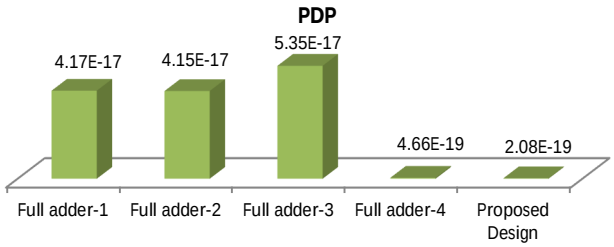

Figure 9. PDP results

CONCLUSION

In this paper, we have presented a new low power full adder cell designs using carbon nanotube field effect transistors. In this design we reduce the number of transistors without resistor and capacitor elements.

Simulation results show a significant improvement in output parameters and finally we showed that we can improve simulation result by reduce the dependence of the output signals.

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