J. Basic. Appl. Sci. Res., 3(7)439-446, 2013
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ISSN 2090-4304
Journal of Basic and Applied Scientific Research
www.textroad.com

Reduction of Leakage Current in Grid Connected Three-Phase PV Inverters

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Abstract

Grid connected inverters have received more attention in power electronic based networks, due to the needless of rechargeable batteries and transformers, resulting in the reduction of size and cost of the systems. On the other hand, the leakage current in such inverters is a critical parameter that should be considered in detail. The leakage current is affected by several parameters, among them common mode voltage plays an important role. As the frequency (variations) of common mode voltage increases, more leakage current will be conducted through the ground. In this paper, a new grid connected three-phase tansformerless inverter is proposed so that the leakage current is reduced by reduction of the frequency of common mode voltage through the zero vectors. The simulations have achieved using the Simpower toolbox of MATLAB software.

KEYWORDS: parasitic capacitor, leakage current, common mode voltage.

1. INTRODUCTION

Solar energy has gradually received more and more attention in research and industry during the last few decades [1].Therefore, the PV power systems, mostly single phase, have gained more applications[2]. Because of the presence of stroke power in the output of single-phase systems, a large DC capacitor is usually necessary in the output circuitry. In three phase systems, however, a small DC capacitor is needed [3], since the output waveform is approximately constant. This leads to an increase in the lifetime and reliability of the systems.

Compared with the other inverters, grid connected inverters have many advantages [4]-[6]. The two common categories of these inverters are embedded transformer and non-embedded transformer. In order to regulate the input DC voltage of the inverter and isolate the PV array from the grid, most of PV systems are embedded transformer inverters. Transformer can be used at line frequency or high frequency. But at line frequency, the transformer is large in size and weight. High frequency transformers used in PV systems are commonly multi-stage transformers. This results in more complexity and losses in the system. Transformerless systems have generally lower cost, size and weight [7]-[9].Moreover, the efficiency of the transformerless topology is about 1 to 2 percent more than that of the embedded transformer topology [10].

Referring to the aforementioned parameters, the transformerless systems are preferred in PV systems. The transformerless system, however, suffers from a serious problem; the PV Arrays are connected to the network without galvanic isolation. As a result, the earth leakage current can be increased through the parasitic capacitors, which are formed between the PV array terminals and the frame, that is normally grounded [11]-[13]. The leakage current can cause several problems in the performance of the system, namely, increasing the grid current distortion, losses, and safety problem [14].

In general, there are two methods to decrease the leakage current via the parasitic capacitor: lowering the voltage amplitude or the frequency through the capacitor .Connecting the capacitor midpoint of the DC linkto the neutral of the grid may be a solution, which includes ahalf-bridgeneutral point clamped(HB-NPC), or a three-phase half-bridge with an extra capacitor connecting the PV array to the neutral of the grid. HB and NPC inverters have high efficiency (above 97%), but because of the extra capacitor, they need a 700V DC link, which is a disadvantage of this topology [15].

Another method is the isolation of the PV array from the grid when the zero vector is applied, which can be implemented either at the ac or at the dc side.

In this paper, a new topology is presented to decrease the variation of common mode voltage. This will lower the leakage current in a three phase transformerless topology. To solve the leakage current problem, the DC link is disconnected from the grid, when the zero vectors are applied to the load. Since the common mode behavior of the system is not influenced by the grid, an ohmic load is used in the simulations of the inverter properties. The proposed topology has a simple LC filter which is adequate and reliable for this system. Because of the low frequency switches, the IGBT transistors can be used to implement this topology.

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1. Common mode voltage

Common mode voltage is a suitable tool to calculate the sum of in-phase voltages into a point. On the other hand, in order to find two voltages with 180ºphase difference, the differential mode voltage is applied. In the present case, our aim is to calculate the potential difference between the PV terminals and the output. From the viewpoint of leakage current, the two terminals of a PV array are the same. Therefore, the common mode voltage is applied between the three-output and one of the PV terminals.

In the q-phase system shown in figure 1, the common mode voltage is obtained with respect to a reference point using the following equation:

$$V_{CM} = \frac{\sum v_{iQ}}{q} \qquad i = 1,2,...,q \tag{1}$$

where i is the number of phases and Q is a reference point of the system (Fig. 1).

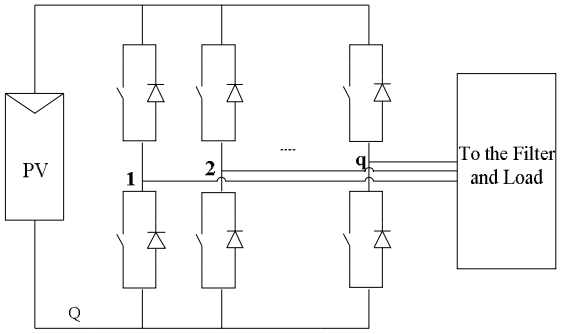


Fig.1.An inverter in q-phase configuration.

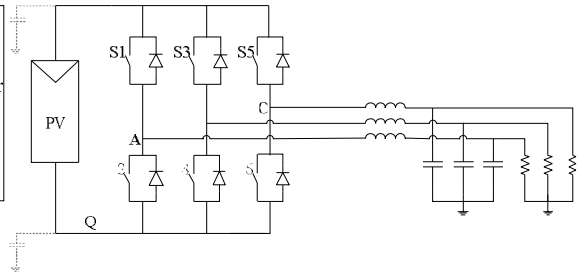


Fig.2. A three-phase inverter topology with parasitic capacitors.

In a three-phase system without neutral connection the three phases are referred to as A, B and C (Fig.2). It is necessary to mention that each switch has 180º phase delay with respect to its coordinate switch and 120º delay to the adjacent switch (Fig. 3). The overlap between the three adjacent switches in this PWM switching scheme, can be used to build up the zero vectors, while the other overlaps can build the active vectors. Fig. 3 shows all the active and zero vectors for this switching method.Forsimplicity, S2, S4, and S6 are not shown in Fig. 3.

This switching strategy, on the other hand, causes variations in the common mode voltage. According to the switch states listed in Table 1, all of the common mode voltage values have been calculated and are indicated in Fig. 3.

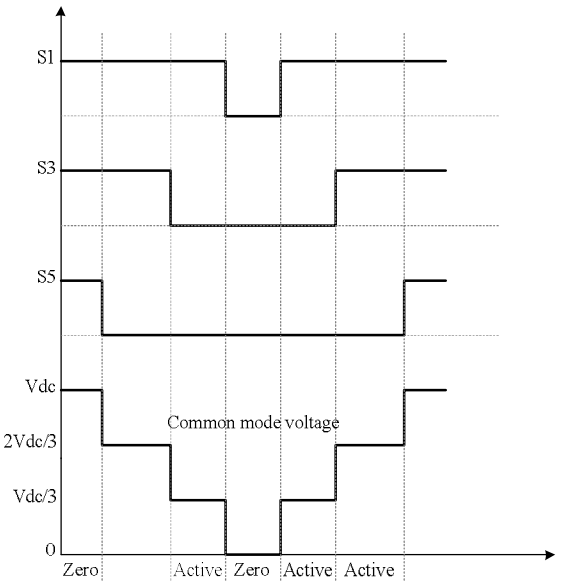
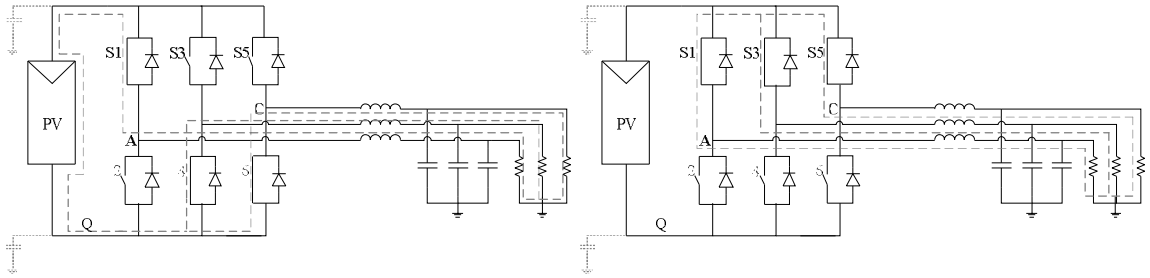


Fig.3. Switching signals and final common mode voltage

Table 1.States of the switches and the corresponding common mode voltage

S1	S3	S5	V_{AQ}	V_{BQ}	V_{CQ}	V_{CM}
0	0	0	0	0	0	0
0	0	1	0	0	V_{DC}	$V_{DC}/3$
0	1	0	0	V_{DC}	0	$V_{DC}/3$
0	1	1	0	V_{DC}	V_{DC}	$2V_{DC}/3$
1	0	0	V_{DC}	0	0	$V_{DC}/3$
1	0	1	V_{DC}	0	V_{DC}	$2V_{DC}/3$
1	1	0	V_{DC}	V_{DC}	0	$2V_{DC}/3$
1	1	1	V_{DC}	V_{DC}	V_{DC}	V_{DC}

This common mode voltage existson both sides of the PV arrays, having a delay relative to each other. It causes leakage current through the parasitic capacitors. Fig. 4 indicates the zero and active states in the three-phase inverter.



(a) (b)

Fig.4.(a)activeand (b)zero vectors current direction of a traditional three-phase inverter

2. Proposed topology

To elicit the common mode voltage from Fig. 2 using MATLAB, the filter has to be made short-circuited. Now, one of the PV array terminals will be the calculated common mode voltage. Fig. 5 is obtained using this method.

All of the simulations are accomplished using Simpower toolbox of the MATLAB software. The time step for the simulations is chosen to be 0.1 μs. The circuit parameters are summarized in Table 2.The output current and voltage are shown in Fig. 6.

Referring to Fig. 3 and Fig. 5, it can be found that the leakage current is too large, since the common mode voltage has large fluctuations. The simulation results have indeed proven the large variations in the common mode voltage. As shown in Fig. 7, the leakage current amplitude is about 5A. This results in an increase in the losses and distortion of the system. In addition, the safety matter should also be considered, which introduces other problems to the system.

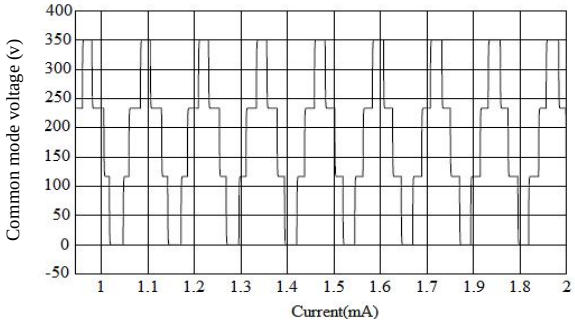


Fig.5.Common mode voltage signal ıl three-phase inverter topology

Table 2.Circuit element values to simulation with MATLAB

Circuit element	Value	description
V_{DC}	350V	PV array voltage
C_{DC}	250µf	DC capacitor
C_P	100nf	Parasitic capacitor between PV array and ground
L_f	1.8mH	Inductance of three phase filter
C_f	2µf	Capacitor of three phase filter
R_{Load}	7.5Ω	Grid load
F_{sw}	8kHz	Switching frequency

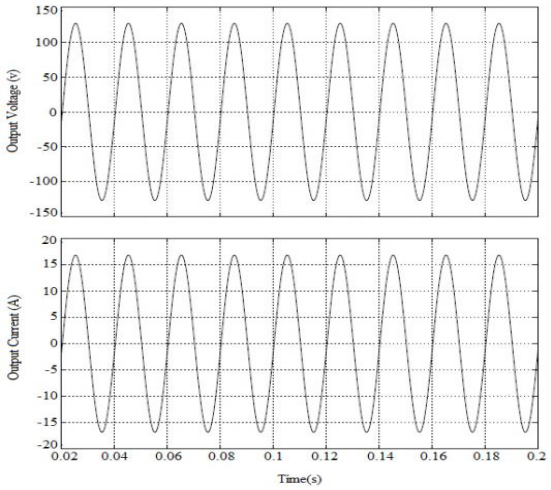


Fig.6.Output voltage and current in the one phase of traditional three-phase inverter

This problem has been investigated and solved in reference [10] for the single phase system. The present work proposes a new topology to decrease the leakage current as much as possible. Table 2 indicates that there are two zero vectors. Applying zero or active vectors causes the common mode voltage to have different levels. The problem is, therefore, to design a strategy to fix the level of the common mode voltages at $V_{DC}/3$ and $2V_{DC}/3$, the levels of the common mode voltage when zero vectors are applied.In this case, the number of common mode voltage levels will decrease to only two levels; and as resultthe leakage current will be decreased. Due to the asymmetrical nature of three-phase inverters, compared with the single phase inverters, this scheme is more difficult to be achieved in three-phase systems.

Here three PV cells are needed to build the voltages of $V_{DC}/3$ and $2V_{DC}/3$. The asymmetrical property requires that every zero vectors to be connected to a separate DC capacitor. The proposed topology is presented in Fig. 8. The bidirectional switches are implemented using diode bridge configuration made by IGBTs. Note that the diodes connected to the DC capacitors are in opposite directions.

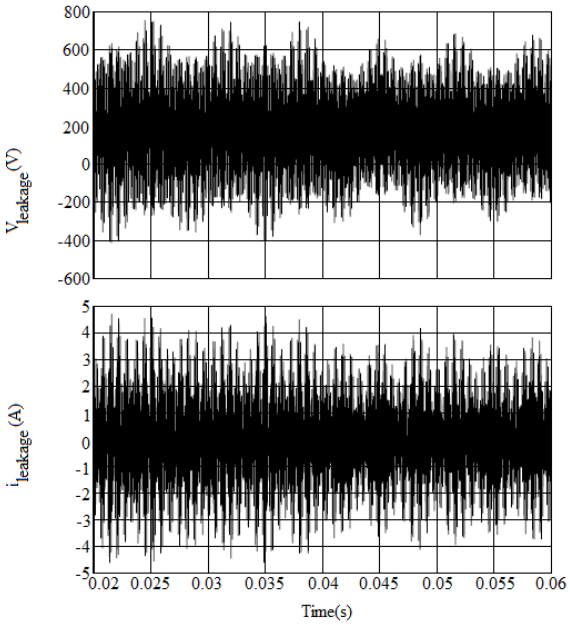


Fig.7. Common mode voltage(voltage of parasitic capacitors) and the leakage current

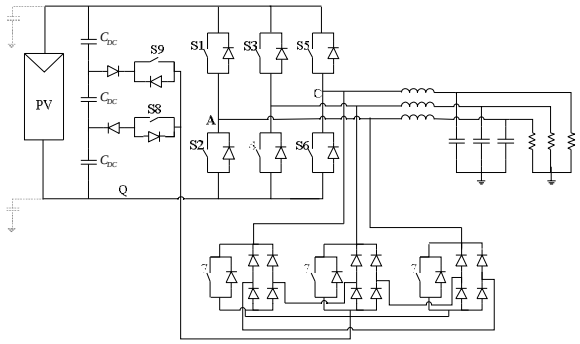


Fig.8. Proposed topology of three-phase PV inverter

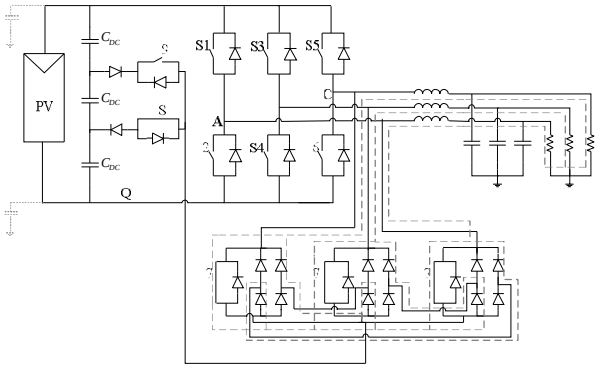


Fig.9.a zero state current direction of proposed topology

According to this topology, by removing these diodes, when a zero vector is applied, the output connects to a specific voltage which is equal to the other levels of the common mode voltage. Due to the asymmetrical property of three-phase inverters compared with single-phase inverters, when a zero vector is applied, the DC capacitor will charge and its voltage will increase. Therefore, the next zero vector will be connected to a voltage different from $V_{DC}/3$ or $2V_{DC}/3$. As a result, a new level will be added to the common mode voltage that leads to an increase in the leakage current. Therefore, if a DC capacitor charges during a time period, this topology forces the capacitor to become discharged in the next period, and the voltage of the DC capacitors will remain constant.Fig. 9 indicates the current path when a zero vector is applied.

Figures 8 and 9 show that at zero state the switches s1 through s6 are open and this situation is accomplished using new switches. A new logic circuit is designed to implement and control the proposed switching strategy. The switching conditions for our strategy are shown in Table 3 and based on this truth table the logic circuit has been designed. In the Table, for simplicity, the switches S2, S4, and S6 are omitted.

Table.3. Truth table of switching of the new three-phase inverter topology and common mode voltage

Old			New									
S1	S3	S5	S1	S3	S5	S7	S8	S9	V_{AQ}	V_{BQ}	V_{CQ}	V_{CM}
0	0	0	0	0	0	1	1	0	$V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$
0	0	1	0	0	1	0	0	0	0	0	V_{DC}	$V_{DC}/3$
0	1	0	0	1	0	0	0	0	0	V_{DC}	0	$V_{DC}/3$
0	1	1	0	1	1	0	0	0	0	V_{DC}	V_{DC}	$2V_{DC}/3$
1	0	0	1	0	0	0	0	0	V_{DC}	0	0	$V_{DC}/3$
1	0	1	1	0	1	0	0	0	V_{DC}	0	V_{DC}	$2V_{DC}/3$
1	1	0	1	1	0	0	0	0	V_{DC}	V_{DC}	0	$2V_{DC}/3$
1	1	1	0	0	0	1	0	1	$V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$

Table 3 implies that the three closed switches (in zero state) will be converted to open state and at the same time three new switches will be closed. Fig. 10 shows the implemented circuit based on Table 3.

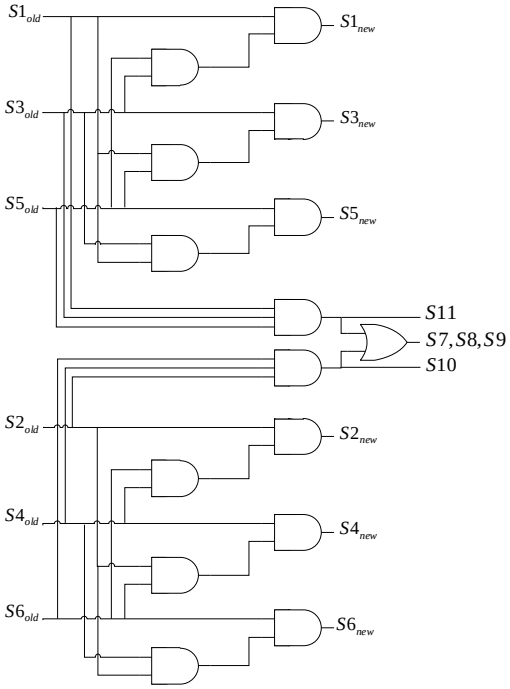


Fig.10.Logic circuit to prepare the switching command of proposed topology

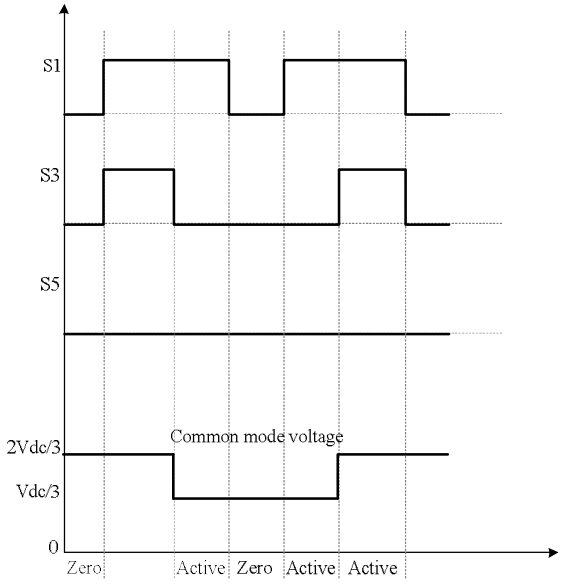


Fig. 11.New switching signals and common mode voltage

By applying the proposed logic circuit to our new topology, the new common mode voltage will have only two levels (Fig. 11). In Fig. 11, the voltage levels V_{DC} and 0 have been eliminated.

As a result, due to the obtained common mode voltage it is expected that the leakage current amplitude will be reduced. Fig.12 shows that the leakage current is indeed decreased to a very low level.

An about 80 percent decrease in the leakage current results in an appreciable reduction in the system losses and an improvement in the safety of the system. The output current and voltage of the proposed topology are shown in Fig. 13. As shown in Fig.13, the output voltage and current remain sinusoidal.

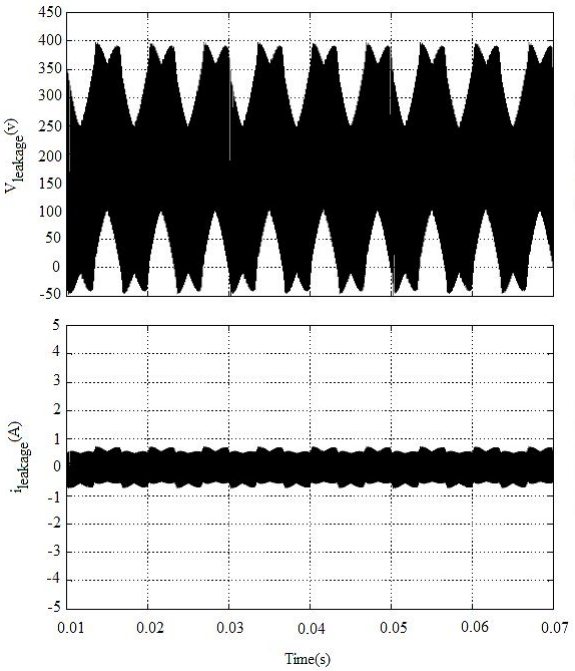


Fig.12.The leakage current and voltage of new topology three-phase inverter

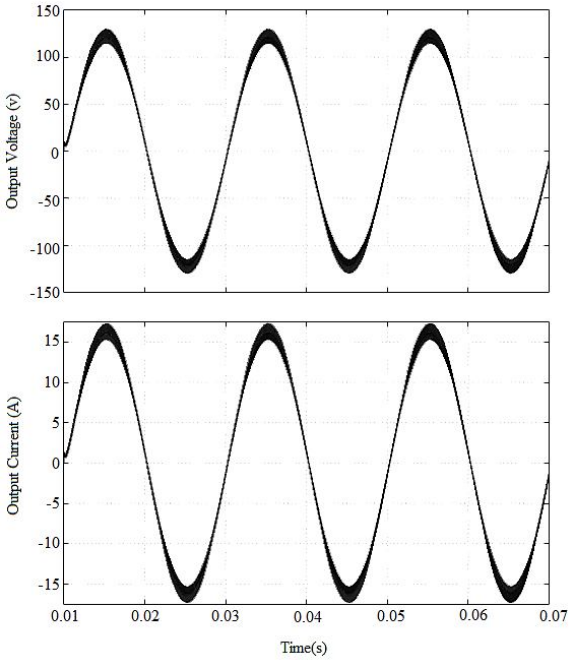


Fig.13.Output current and voltage of the proposed three-phase inverter

3. Conclusion

The leakage current is a significant issue in theadvanced power systems. Invertersplay an important role in these power-electronic-based systems. In this paper, a new topology for three-phase inverters has been introduced. The simulation results show an 80% decrease in the leakage current for the proposed model. In the model, the switching frequency is equal to, or even lower than, the switching frequency used in the traditional systems. Therefore, the switching speed is not a problem in the proposed topology as this is another advantage of our model. The simulations of the traditional and proposed inverters have been achieved using the Simpower toolbox of the MATLAB software with 0.1μs time steps.

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