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An Improve Current Mode OR\ NOR Circuits Design with Temperature Independency in Range (0 to 100)

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ABSTRACT

In many applications, device speed is the most important requirement, and so conventional voltage mode silicon based devices cannot solve this necessity. Many years ago the current mode logic is proposed as a potential solution for this problem but combining this logic and MOSFET technology reduces the speed advantage pertains to the current mode logic and furthermore have additional imperfection due to using MOSFET technology. By using current mode logic we have achieved a significant improvement in the circuit parameters such as delay and power delay product. This paper presents an efficient circuit designs for OR-NOR logical functions in the current mode and MOSFET technology. The circuits being studied are optimized for energy efficiency at 0.13u CMOS technology. HSPICE is used to simulate these circuits. The denouements, that we have achieved, show the best performance in the different Temperature (0 to 100) in comparison with the state of the art designs.
KEYWORDS:MOSFET technology, Multiple-valued logic, OR/ NOR logic functions.

1. INTRODUCTION

By the explosive growth in laptops, portable personal communication systems and the evolution of the shrinking technology, the research effort in low-power microelectronics has been improved and low-power VLSI systems have emerged as highly in demand. Nowadays, there are an increasing number of portable applications requiring small-area low-power high- throughput circuitry. Hence, circuits with low power consumption become the major candidates for design of microprocessors and system-components [1,3]. The battery technology does not advance at the same rate as the microelectronics technology and there is a limited amount of power available for the mobile systems [2,4,7]. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not necessarily imply low energy [6]. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation .Therefore, designers are faced with more constraints such as high speed, high throughput, small silicon area and at the same time low power consumption. In many applications, device speed is the most important requirement, and so conventional voltage mode silicon based devices cannot solve this necessity [9,5]. Many years ago the current mode logic is proposed as a potential solution for this problem but combining this logic and MOSFET technology reduces the speed advantage pertains to the current mode logic, and furthermore have additional imperfection due to using MOSFET technology. In recent years, this technology has been entered in nano scale region as continues to scale deeper into the nano scale, device non idealities cause I-V characteristics to be substantially different from well tempered MOSFETs that increase the deficiencies of using silicon based technology [7,8].

2. The common gates of current mode

Due to its circuit techniques, the current mode has become an integral part of analog integrated circuits and its critical design in speed and power consumption competes against each other. Because of its unique characteristics, among which the algebraic sum is one of the best, it can be used to present new designs with changing numbers of import, the capability to control the threshold detector in order to implement the multiple-valued logic function, current mode analog multipliers which are used as main block frequency synchronizers and active parallel systems, implementing number systems and different fields, such as resiude number systems and galo is field. In comparison with voltage type the noise level in current mode will be less, due to similar power supplies. However, the temperature which is mistakenly discussed as noise in some books and papers, is one of the most

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effective elements on the characteristic curve and even on current mode circuit functions. In some functions, such as OR, the thermal effect may influence the characteristic effect and raise the deviation from the evaluation criteria, but in some other functions, such as AND and XOR, the thermal effect will influence the overall function of the circuit.

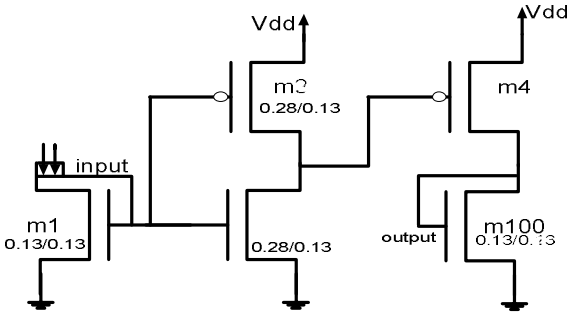


Fig . 1. OR common circuit

3. The thermal effect on the common gates of the current mode

Generally, any changes in temperature will greatly decrease both Vt and μ parameters. A decrease in Vt leads to a raise in Id and a decrease in μ leads to a decrease in Id . However, because of μ exponential curve drop, a raise in temperature and heat, and common functions of electronic devices (-20 to 100 cel degrees) will finally decrease the current in this transistor. In Fig.2, the characteristic curve of an OR common gate (fig.1) with temperature switching is demonstrated in three temperatures of -20, 37 and 100 cel degrees.

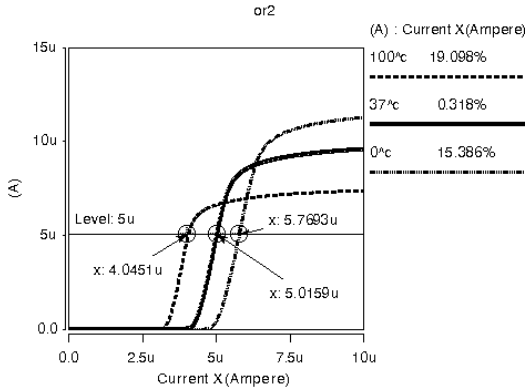


Fig . 2. OR common circuit function

4. The introduction of evaluation criteria and deviation from the evaluation criteria

In order to study the functions of a logical gate, we need to control and compare the present parameters, in a way that if one function is close to optimal function, we will describe it as the optimal circuit and logical gate. In this paper, we have tried to describe a criteria to be the optimal criteria related to its logical gate, the greatness of criteria deviation which describes the 100 % optimal function, the amount of a circuit to be optimal and the percent of circuit optimal function deviation as a number whose greatness indicates the deviation from the optimal function or non-deviation from the circuit optimal criteria.

If we describe three logical values as 0, 1, and 2, the greatest current which is implemented on the circuit must be specified to the highest logical value,2, and the lack of current will describe the zero logical value. The best value that can be specified to 1, is the value that has the highest and symmetric possible distance from 0 and 2, then I_{ref} can be defined as the most optimal logical value.

To control the logical values and to describe the logical gates by different circuits, the threshold which shows the border between two logical values will be needed and the border between two logical values must be at the highest possible distance and symmetric to both values.

Thus, the most optimal threshold between 0 and 1 could be $(0 + I_{ref}) / 2 = I_{ref}/2$ and the most optimal threshold between 1 and 2 could be $(I_{ref}+2I_{ref}) / 2 = 3\ I_{ref}/\ 2$ and the high threshold criteria can be known as the most optimal threshold bet 1 and 2, and equal to $3\ I_{ref}/\ 2$ and the low

threshold criteria can be described as the most optimal threshold between 0 and 1 and equal to I_{ref}/ 2. Now, by comparing the presented gate with its related criteria, it can be discovered whether the criteria is optimal or not. In this direction, in order to have the same criteria for all present logics to compare their function, a deviation as the deviation from evaluation criteria which describes the deviation rate from evaluation criteria in each logical gate has been defined,. Here, we describe them as following.

($\eta = 1 -$ Threshold current in the gate being tested /evaluation criteria)

This deviation has been achieved in return for the threshold s which are needed to describe one logical value and in the case of needing more than one threshold, it will be described by threshold deviation mean.

5. The introduction of suggested OR and NOR gates

The logical function of OR and NOR will be as following. (table 1)

Table 1: OR and NOR Logical function

	or	*nor*
0	0	1
1	1	0
2	1	0

As it is obvious, only one threshold is needed to separate 0 and 1. Thus, we need one low threshold criteria to distinguish the suggested circuit function and to describe the deviation. Deviation in OR and NOR could be computed based on:

($\eta = 1 -$ the threshold current in the gate being tested * 2/ I_{ref}) (1)

The suggested circuit to describe OR will be like fig.3. The suggested circuit function to describe OR in different temperatures will be shown in fig.4.(It must be mentioned that the M100 transistor is located at the exit point so that according to the shape of entering elements, it can control the load effect at the exit point. In this paper, in all presented new circuits , it is used as the controller of load effect.)

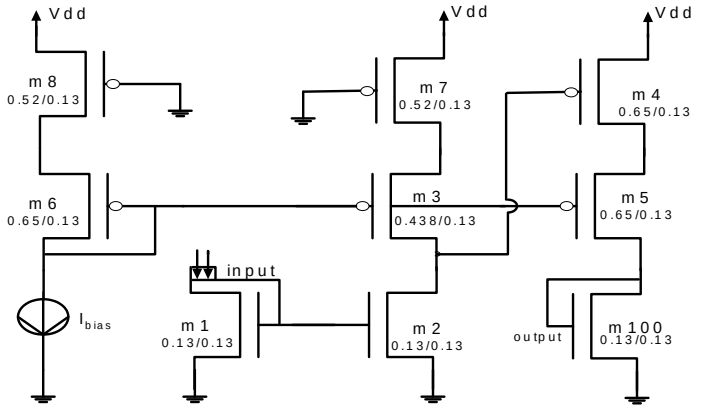


Fig. 3. OR suggested circuit

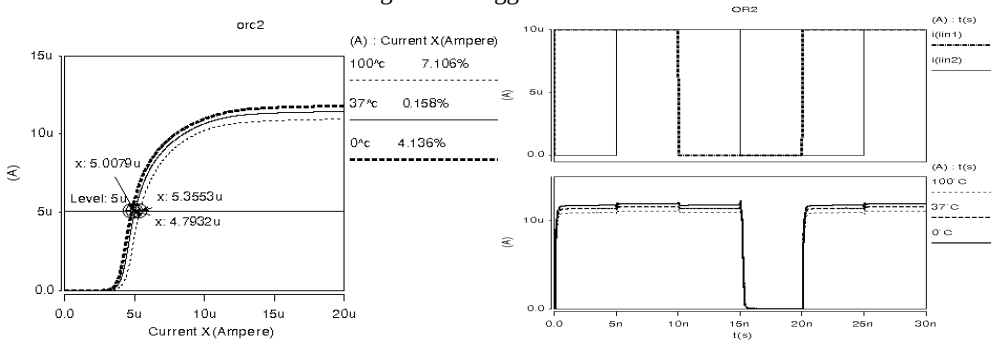


Fig . 4. The function of suggested circuit OR

As it is shown in the picture, instead of power source control and accordingly different logic functions, W/L relation control has been used to achieve the current which is needed for different logic functions from a fixed current. This function will decrease the thermal effect on the circuits and will have a smaller area for optimal thermal switching. The suggested circuit to describe NOR will be like Fig.5.

Fig. 6, shows the suggested circuit function to describe OR in different temperatures and the deviation rate as well. In this design, the m9 and m10 transistors are added to the circuit which present a NOT function and by this feature control the m4.

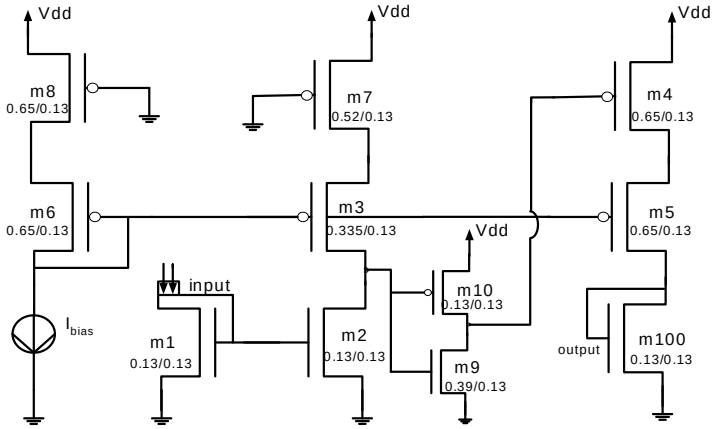


Fig. 5. NOR suggested circuit

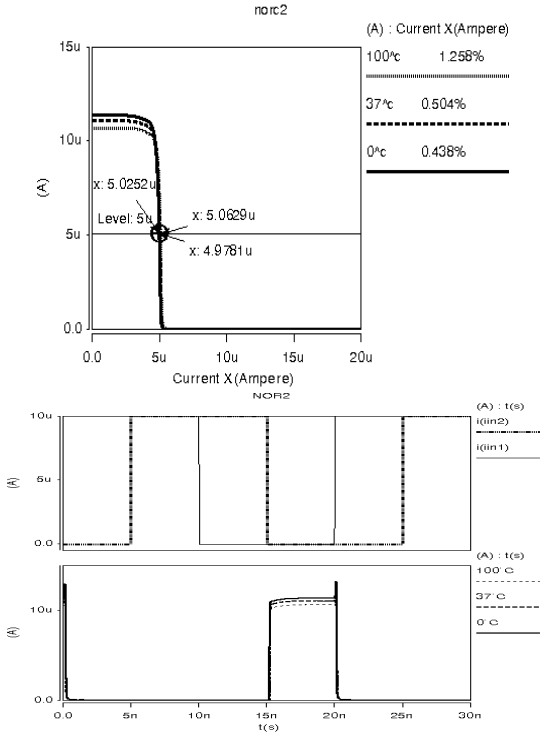


Fig . 6. NOR suggested circuit function

6. Time simulation of suggested gates and the study of deviation in different temperatures

In table 2, the time simulation results of two suggested gates and deviation rate in three temperatures [0, 37,100] is presented. (In fig.7, The time simulation results is presented.)

Table 2: Time simulation

	Or	Nor
0℃	4.136%	0.438%
37℃	0.158%	0.504%
100℃	7.106%	1.258%

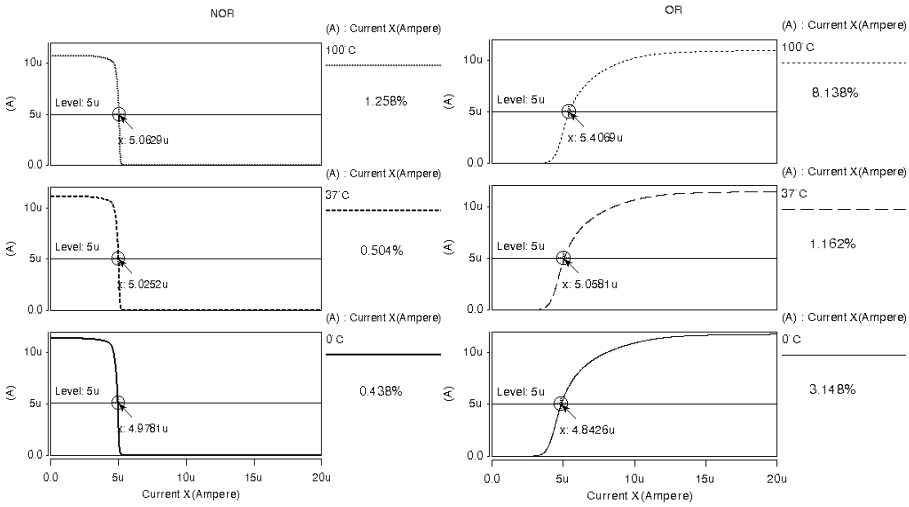


Fig.7. Time simulation results and deviation rate

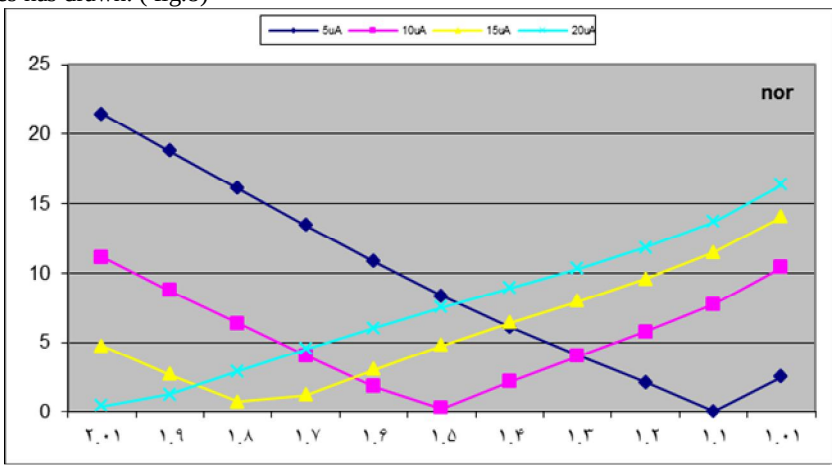
7. The comparison of suggested gates deviation in different temperatures with common gates in the same conditions

As the pictures indicate, the deviation rate in voltage limits of 2 to 1 is obtained and if the deviation less than 10 % is considered as the optimal deviation , the lowest and the highest optimal voltage which provide the optimal deviation rate in different currents are presented in Table 3.

Table 3: Gates function optimal voltage limits based on BIOS current

	OR		NOR	
=<10%	min	Max	min	max
5uA	1.2105	1.3674	1.0000	1.5666
10uA	1.3997	1.603	1.0157	1.9531
15uA	1.5587	1.8036	1.1778	2.0000
20uA	1.7048	1.9925	1.3235	2.0000

The output of gates function based on BIOS current at different temperatures and different voltages has drawn. (fig.8)



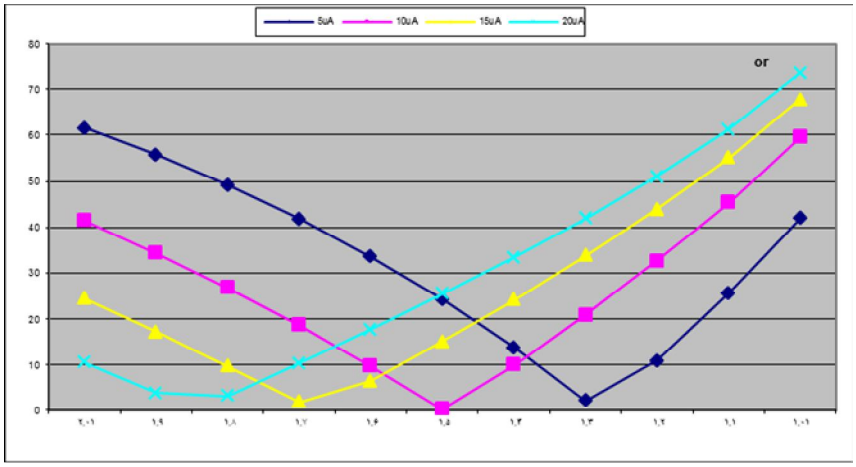


Fig . 8. Charts of simulation results

8. Conclusion

In this paper two circuits and their results in the current mode logic have been proposed. The proposed circuits by using the CMOS technology have a significant improvement in the circuit parameters such as delay and power delay product. simulation have been performed on HSPICE by using 0.13u technology and its results shows that the present circuits have better standard deviation than the previous circuits with the current mode logic. In comparison with the state of the art circuit designs in the different temperatures, our proposed circuit's standard deviation is 1.25% at the range of 0 to 100.

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